XVME-976

Adapter Module

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Chapter 1 - Introduction

Overview

The XVME-976 adapter module provides I/O expansion for Xycom's XVME-654 and XVME-655 VMEbus PC/AT processor modules. Direct connection is possible with the XVME-654. Connections with the XVME-655 require a transition board, such as the XVME-978/1 Ethernet card, or XVME-978/100 transition module, which plug into the XVME-655 and provide the mechanical and electrical connections for the XVME-976.

Module Features

The XVME-976 offers the following features:

- One PC/104 and one PMC expansion module site
- On-board DC regulator to supply 3.3 volts to the PMC site
- Pin and socket connector scheme
- Optional PC/104-compatible modules for Ethernet, SCSI, serial and parallel expansion (available from Xycom)
- Optional PMC modules (available through third party) for ATM, FDDI and SCSI expansion

Expansion Modules

Minimal configuration for an expanded system includes:

- VMEbus processor module (the XVME-654 or XVME-655 with XVME-978/1 or 978/100)
- XVME-976 adapter module
- PC/104 or PMC expansion module

PC/104 Expansion Modules

The PC/104 expansion site on the XVME-976 allows PC/104 compatible modules to be used with XVME-654/655. These signals arrive from the host XVME-PC/AT. PC/104 expansion modules provide various I/O functions such as: Ethernet, SCSI, serial, parallel and flash disk.

Two types of PC/104 expansion modules can be used with the XVME-976 adapter module:

- Type A – Xycom PC/104 module with integral front panel included; mechanical dimensions of 4.010” x 5.091”
- Type B – Generic PC/104 module; mechanical dimensions of 3.550” x 3.775” (may require additional front panel kit)

PCI Mezzanine Card (PMC) Expansion Modules

The XVME-976 provides a PCI Mezzanine Card (PMC) site that allows the PCI functionality of the XVME-654 and -655 to be expanded. Electrically equivalent to the PCI bus standard, PMC has been adopted by VMEbus International Trade Association (VITA) and the VMEbus community to expand the PCI capability of the VMEbus processor modules. The PMC site on the XVME-976 supports PMC J2 I/O options.

Processor Connection Options

The XVME-976 supports connections to the XVME-654 and XVME-655 VMEbus PC/AT processor modules.

Installing the XVME-976 on an XVME-654

The adapter module connects directly to the XVME-654 via Interboard Connectors 1 and 2. Additional equipment (supplied with the XVME-976) needed to complete the connection is as follows:

- Two corner standoffs
- Two pairs of standoff screws

Installing the XVME-976 to the host XVME-654 Processor Module

1. Follow procedures for the prevention of static discharge to prevent damage to the circuitry of the modules.
2. Disconnect all power sources.
3. Loosen the screws on the front panel of the XVME-654 processor module.
4. Remove the XVME-654 from the VME backplane, as follows:
    - Gently pull on the face plate until it slides out of the chassis

5. Place the XVME-654 on a static-free surface with the Interboard connectors facing up.
6. Align interboard connectors 1 and 2 on the XVME-976 with the same connectors on the XVME-654.
7. Gently press the two boards together. *Do not bend or twist the XVME-976.*
8. Add standoffs (2) and standoff screws (2 pairs) as illustrated in Figure 1-1.

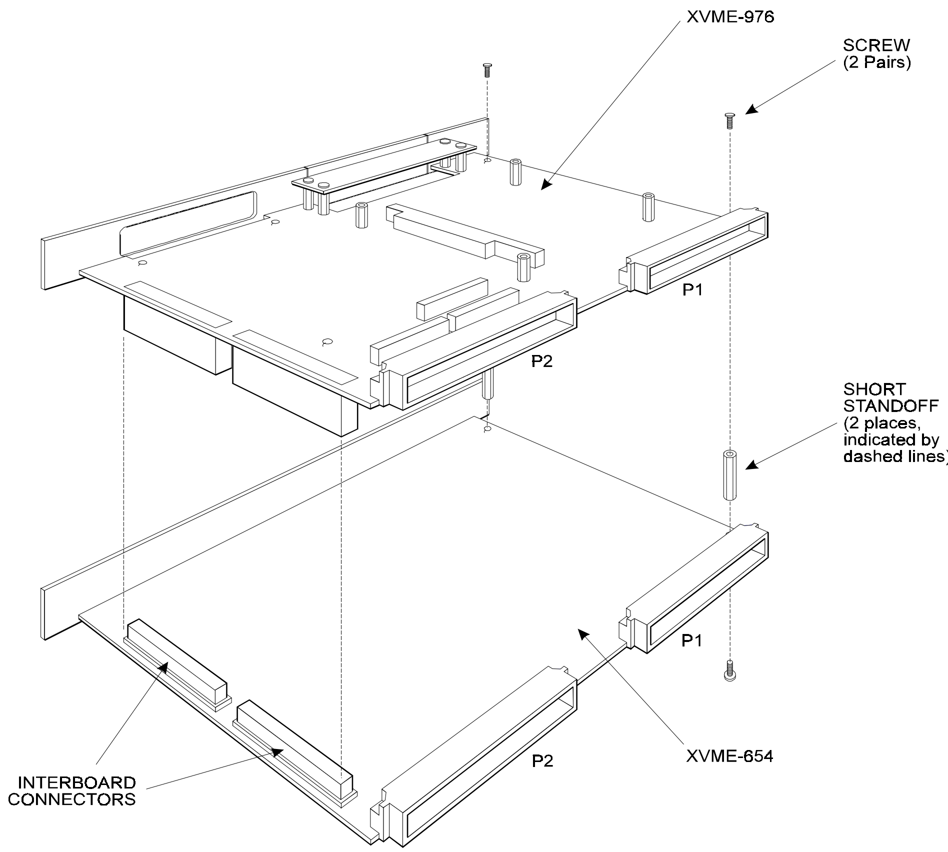

Figure 1-1. Installing XVME-976 onto XVME-654

9. Clear two adjacent card cage slots.
10. Align the two connected modules (with the XVME-976 on the right) on the card guides in the slots.
11. Gently push the modules to the rear of the chassis until the P1 and P2 connectors engage.
12. Tighten the screws on the front panel of the XVME-654 processor module to secure the connected modules into place. *The installation is complete.*

Installing the XVME-976 on an XVME-655

The XVME-976 connects to the XVME-655 indirectly through an XVME-978 expansion module. Additional equipment needed to complete the connection is as follows:

- Two long standoffs, and either the
- XVME-978/1 Ethernet expansion module or the
- XVME-978/100 transition module (if Ethernet functionality is not needed)

Installing the XVME-976 to the Host XVME-655 Processor Module

Note

This procedure assumes the XVME-978 has been installed onto the XVME-655 processor module. Instructions for installing the XVME-978 onto the XVME-655 can be found in the XVME-655 manual.

1. Follow procedures for the prevention of static discharge to prevent damage to the circuitry of the modules.
2. Disconnect all power sources.
3. Loosen the screws on the front panel of the XVME-655 processor module.
4. Remove the XVME-655 (with XVME-978 connected) from the VME backplane, as follows:
   - Gently pull on the face plate until it slides out of the chassis
5. Place the boards on a static-free surface with the XVME-978 on top.
6. Align interboard connectors 1 and 2 on the XVME-976 with the interboard connectors on the XVME-978 module.
7. Gently press the two boards together. *Do not bend or twist the XVME-976.*
8. Add standoffs (2) and standoff screws (2 pairs) as illustrated in Figure 1-2.

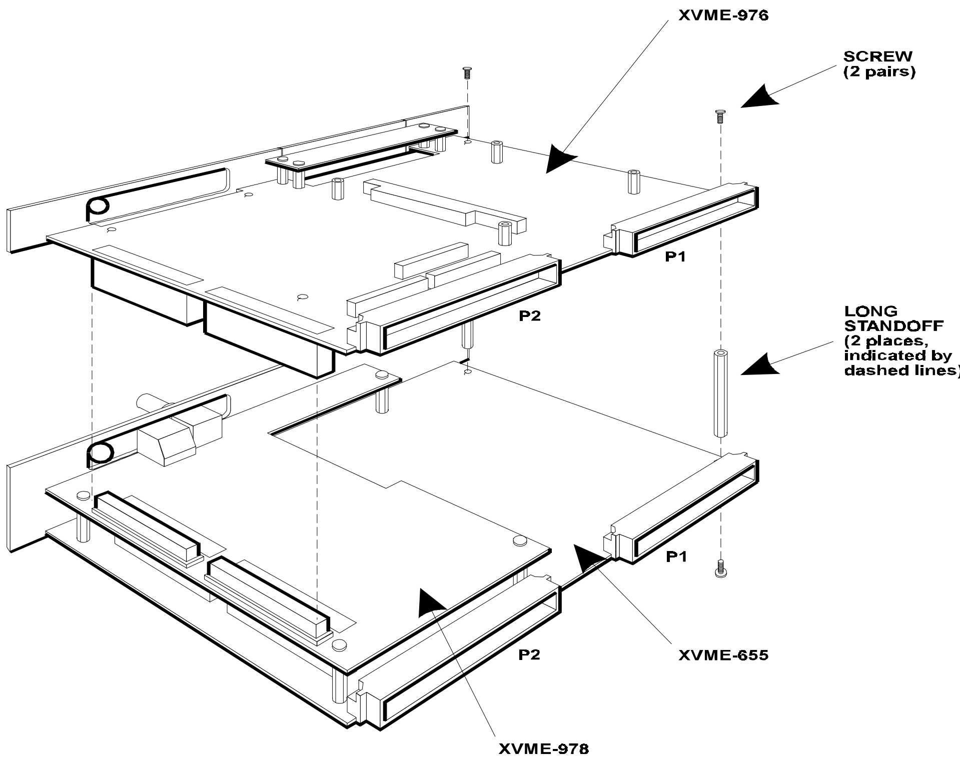

Figure 1-2. Installing XVME-976 onto XVME-978

9. Clear three adjacent card cage Slots.
10. Align the three connected modules (with the XVME-976 on the right) on the plastic guides in the slots.
11. Gently push the modules to the rear of the chassis until the P1 and P2 connectors engage.
12. Tighten the screws on the front panel of the XVME-655 processor module to secure the connected modules into place. *The installation is complete.*

PC/104 Module Installation

The following types of PC/104 expansion modules can be mounted to the XVME-976:

- Xycom's Type A (PC/104) expansion modules
- Generic Type B (PC/104) expansion modules
- PMC expansion modules

The following sections explain the installation procedures for mounting PC/104-compatible (Types A and B) expansion modules onto an XVME-976 adapter module.

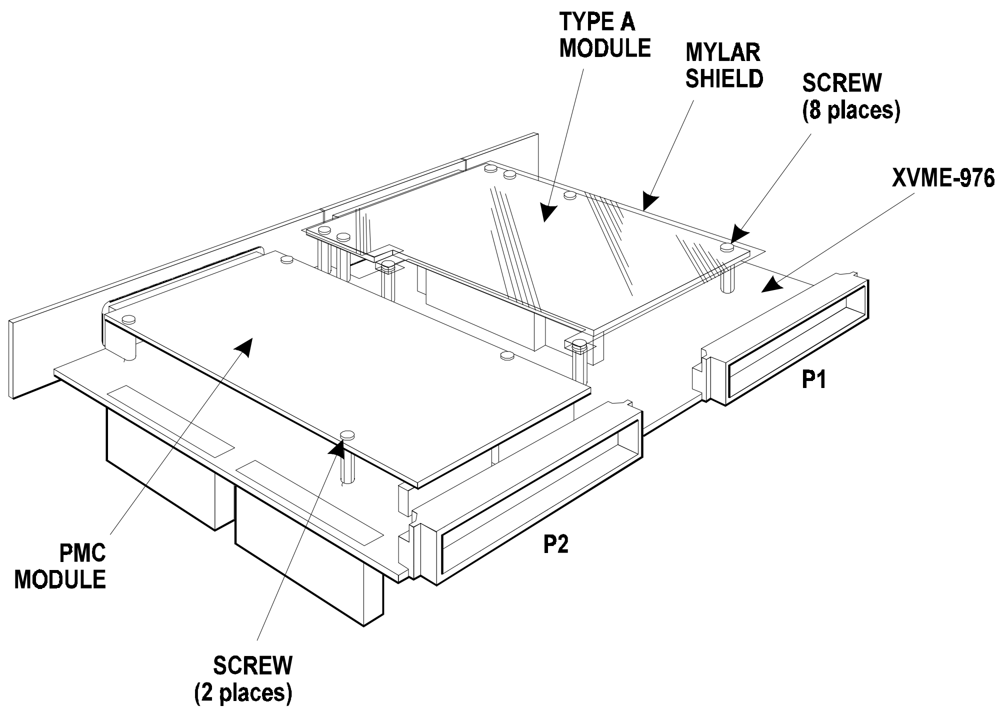

Figure 1-3. XVME-976 with PMC and Type A (4.010 x 5.091") Modules

Type A Module Installation

The XVME-976 is configured to accept the installation of Xycom's Type A module in the PC/104 site. Type A modules contain a front panel that is attached to the circuit board. Additional equipment included for the connection of the two modules:

- Six standoffs
- Eight nylon screws (connects the corners of the module to the XVME-976)

Installing the Type A Module onto the XVME-976 Adapter Module

> **Note**
>
> This procedure assumes the XVME-976 is attached to either the XVME-654 or XVME-655 module. Procedures for installing the XVME-976 onto those modules can be found earlier in this chapter.

1. Follow procedures for the prevention of static discharge to prevent damage to the circuitry of the modules.
2. Disconnect all power sources.
3. Loosen the screws on the front panel of the XVME processor module.
4. Remove the XVME-976 and any attached modules from the VME backplane, as follows:
    - Gently pull on the face plate(s) until the board(s) slide out of the chassis
5. Place the XVME-976 (and any attached boards) on a static-free surface with the XVME-976 on top. See Figure 1-3.
6. Remove four screws securing the blank front panel assembly from the XVME-976 (set aside for later).
7. Remove the blank front panel assembly from XVME-976 (save for possible future use).
8. Remove the four screws securing the mylar shield. Be sure to retain the screws for use in securing the PC/104 module to the XVME-976.
9. Remove the mylar shield from the XVME-976 PC/104 site (save for future use).
10. Install the new mylar shield that came with the Type A expansion board.
11. Insert two screws on the standoffs, adjacent to the PC/104 connector, to secure the mylar shield.
12. Fold the mylar shield up to allow expansion module installation.

13. Align the PC/104 connectors of the XVME-976 with the corresponding connectors on the Type A module.
14. Gently press the two boards together. *Do not bend or twist the XVME-976.*
15. Fold the mylar shield down.
16. Install the remaining screws to secure the Type A module.
17. Align the three connected modules (with the Type A module on the right) on the plastic guides in the slots leading to the VME backplane.
18. Gently push the modules to the rear of the chassis until the P1 and P2 connectors engage.
19. Tighten the screws on the front panel of the XVME processor module to secure the connected modules into place. *The installation is complete.*

Type B Module Installation

The XVME-976 is configured to accept the installation of generic Type B modules in the PC/104 site. Type B modules contain cable connectors may require a Xycom front panel kit. Additional equipment included or required for connecting a Type B module to the XVME-976:

- Xycom front panel kit
- Six standoffs
- Two nylon screws (secures the module to the XVME-976)
- Four nylon screws (secures the front panel to the XVME-976)

Note

Type B modules purchased from Xycom will include a front panel kit. PC/104 modules purchased from a third party will *not* contain front panel kits compatible with the XVME-976.

Installing Type B Module onto the XVME-976 Adapter Module

Note

This procedure assumes the XVME-976 is attached to either the XVME-654 or XVME-655 module. Procedures for installing the XVME-976 onto those modules can be found earlier in this chapter.

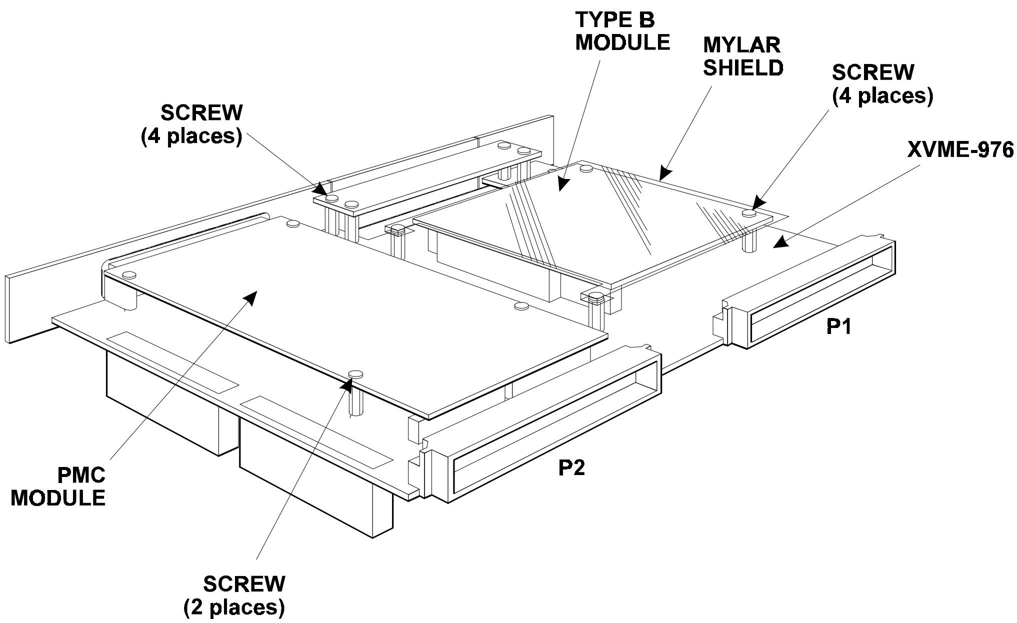

Figure 1- 4. XVME-976 with Type B (3.550" x 3.775") and PMC Modules Installed

1. Follow procedures for the prevention of static discharge to prevent damage to the circuitry of the modules.
2. Disconnect all power sources.
3. Loosen the screws on the front panel of the XVME processor module.
4. Remove the XVME-976 and any attached modules from the VME backplane, as follows:
   - Pull gently on the face plate(s) until the board(s) slide out of the chassis
5. Place the XVME-976 (and any attached boards) on a static-free surface with the XVME-976 on top. See Figure 1-3.
6. Remove four screws securing the blank front panel assembly from the XVME-976 (set aside for later).

7. Remove blank front panel assembly from XVME-976 (save for possible future use).
8. Connect the cables from the front panel kit to the Type B expansion module.
9. Remove the two screws opposite the PC/104 connector and fold the mylar shield back to expose the standoffs. Be sure to retain the screws for use in securing the PC/104 module to the XVME-976.
10. Align the PC/104 connectors of the XVME-976 with the corresponding connectors on the Type B module.
11. Gently press the two boards together. *Do not bend or twist the XVME-976.*
12. Fold the mylar shield down (over the solder side of the expansion module).
13. Insert the two screws removed in Step 9.
14. Attach the new front panel assembly, if provided, to the XVME-976 with the four screws removed in Step 6.
15. Align the connected modules (with the XVME-976 on the right) on the plastic guides in the slots.
16. Gently push the modules to the rear of the chassis until the P1 and P2 connectors engage.
17. Tighten the screws on the front panel of the XVME processor module to secure the connected modules into place. *The installation is complete.*

PMC Module Installation

The XVME-976 is designed to accept the installation of PMC expansion modules to add PCI functionality.

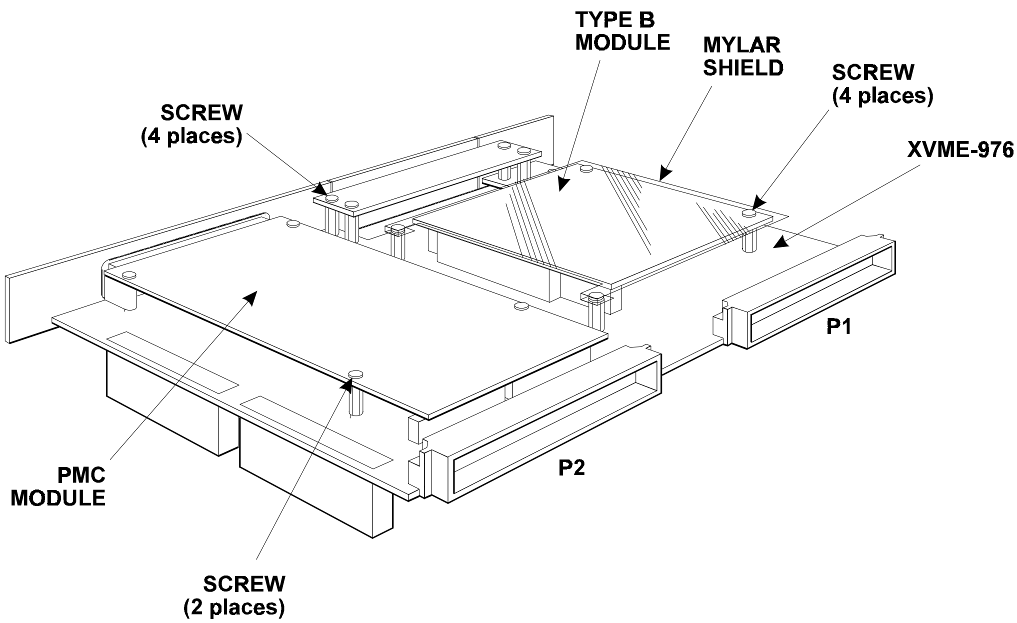

Figure 1-5. XVME-976 with PMC Expansion Module

> **Note**
>
> The XVME-976 PMC site is keyed to accept only 5-volt boards. Other voltage configurations will not fit on this site.

Installing the PMC Module onto the XVME-976 Adapter Module

> **Note**
>
> This procedure assumes the XVME-976 is attached to either the XVME-654 or XVME-655 module. Procedures for installing the XVME-976 onto those modules can be found earlier in this chapter.

1. Follow procedures for the prevention of static discharge to prevent damage to the circuitry of the modules.
2. Disconnect all power sources.
3. Loosen the screws on the front panel of the XVME processor module.
4. Remove the XVME-976 and any attached modules from the VME backplane, as follows:
    - Gently pull on the face plate(s) until the board(s) slide out of the chassis
5. Place the XVME-976 (and any attached boards) on a static-free surface with the XVME-976 on top. See Figure 1-5.
6. Pop out the filler plate in the XVME-976 front panel.
7. Align the PMC board with the 5-volt key. See Figure 1-5.
8. Insert the four screws to secure the expansion module to the XVME-976.
9. Align the connected modules (with the XVME-976 on the right) on the plastic guides in the slots.
10. Gently push the modules to the rear of the chassis until the P1 and P2 connectors engage.
11. Tighten the screws on the front panel of the XVME processor module to secure the connected modules into place. *The installation is complete.*

Connectors

The following tables contain pinout information for the various XVME-976 connectors:

PC/104 Connector Pinouts

Table 1-1. PC/104 Connector Pinouts

Pin	Row A (P3)	Row B (P3)	Row D (P4)	Row C (P4)
0	-	-	GND	GND
1	IOCHCK*	GND	MEMCS16*	SBHE*
2	SD7	RESETDRV	IOCS16*	LA23
3	SD6	+5V	IRQ10	LA22
4	SD5	IRQ9	IRQ11	LA21
5	SD4	NC	IRQ12	LA20
6	SD3	DRQ2	IRQ15	LA19
7	SD2	-12V	IRQ14	LA18
8	SD1	NC	NC	LA17
9	SD0	+12V	NC	MEMR*
10	IOCHRDY	NC	DACK5*	MEMW*
11	AEN	SMEMW*	DRQ5	SD8
12	SA19	SMEMR*	DACK6*	SD9
13	SA18	IOW*	DRQ6	SD10
14	SA17	IOR*	NC	SD11
15	SA16	NC	NC	SD12
16	SA15	NC	+5V	SD13
17	SA14	DACK1*	NC	SD14
18	SA13	DRQ1	GND	SD15
19	SA12	REF*	GND	NC
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5V		
30	SA1	OSC		
31	SA0	GND		
32	GND	GND		

PMC Expansion Site Connector Pinouts

Table 1-2. J-11 Pinouts

Pin	Name	Pin	Name
1	TCK	2	-12V
3	GND	4	INTA*
5	INTB*	6	INTC*
7	BUSMODE1*	8	+5V
9	INTD*	10	PCI-RSVD14B
11	GND	12	PCI-RSVD
13	CLK	14	GND
15	GND	16	GNT*
17	REQ*	18	+5V
19	V I/O	20	PAD(31)
21	PAD(28)	22	PAD(27)
23	PAD(25)	24	GND
25	GND	26	C BE3*
27	PAD(22)	28	PAD(21)
29	PAD(19)	30	+5V
31	V I/O	32	PAD(17)
33	FRAME*	34	GND
35	GND	36	IRDY*
37	DEVSEL*	38	+5V
39	GND	40	PLOCK*
41	SDONE	42	SBO
43	PAR	44	GND
45	V I/O	46	PAD(15)
47	PAD(12)	48	PAD(11)
49	PAD(9)	50	+5V
51	GND	52	C BE0*
53	PAD(6)	54	PAD(5)
55	PAD(4)	56	GND
57	V I/O	58	PAD(3)
59	PAD(2)	60	PAD(1)
61	PAD(0)	62	+5V
63	GND	64	REQ64*

Table 1-3. J12 Pinouts

Pin	Name	Pin	Name
1	+12V	2	TRST*
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	PCI-RSVD*
9	PCI-RSVD*	10	PCI-RSVD*
11	BUSMODE2*	12	+3.3V
13	RST*	14	BUSMODE3*
15	+.3V	16	BUSMODE4*
17	PCI-RSVD*	18	GND
19	PAD(30)	20	PAD(29)
21	GND	22	PAD(26)
23	PAD(24)	24	+3.3V
25	IDSEL	26	PAD(23)
27	+3.3V	28	pad(20)
29	PAD(18)	30	gnd
31	PAD(16)	32	C_BD2*
33	GND	34	PMC-RSVD
35	TRDY*	36	+3.3V
37	GND	38	STOP*
39	PERR*	40	GND
41	+3.3V	42	SERR*
43	C_BD1*	44	GND
45	PAD(14)	46	PAD(13)
47	GND	48	PAD(10)
49	PAD(8)	50	+3.3V
51	PAD(7)	52	PMC-RSVD
53	+3.3V	54	PMC-RSVD
55	PMC-RSVD	56	GND
57	PMC-RSVD	58	PMC-RSVD
59	GND	60	PMC-RSVD
61	ACK64*	62	+3.3V
63	GND	64	PMC-RSVD

Table 1- 4. J14 Pinouts

Pin	Name	Pin	Name
1	USER I/O - 1	2	USER I/O - 2
3	USER I/O - 3	4	USER I/O - 4
5	USER I/O - 5	6	USER I/O - 6
7	USER I/O - 7	8	USER I/O - 8
9	USER I/O - 9	10	USER I/O - 10
11	USER I/O - 11	12	USER I/O - 12
13	USER I/O - 13	14	USER I/O - 14
15	USER I/O - 15	16	USER I/O - 16
17	USER I/O - 17	18	USER I/O - 18
19	USER I/O - 19	20	USER I/O - 20
21	USER I/O - 21	22	USER I/O - 22
23	USER I/O - 23	24	USER I/O - 24
25	USER I/O - 25	26	USER I/O - 26
27	USER I/O - 27	28	USER I/O - 28
29	USER I/O - 29	30	USER I/O - 30
31	USER I/O - 31	32	USER I/O - 32
33	USER I/O - 33	34	USER I/O - 34
35	USER I/O - 35	36	USER I/O - 36
37	USER I/O - 37	38	USER I/O - 38
39	USER I/O - 39	40	USER I/O - 40
41	USER I/O - 41	42	USER I/O - 42
43	USER I/O - 43	44	USER I/O - 44
45	USER I/O - 45	46	USER I/O - 46
47	USER I/O - 47	48	USER I/O - 48
49	USER I/O - 49	50	USER I/O - 50
51	USER I/O - 51	52	USER I/O - 52
53	USER I/O - 53	54	USER I/O - 54
55	USER I/O - 55	56	USER I/O - 56
57	USER I/O - 57	58	USER I/O - 58
59	USER I/O - 59	60	USER I/O - 60
61	USER I/O - 61	62	USER I/O - 62
63	USER I/O - 63	64	USER I/O - 64

Table 1-5. VME P2 Connector Pinouts

Name	Pin	Name	Pin	Name	Pin
A1	USER I/O - 2	B1	VCC	C1	USER I/O - 1
A2	USER I/O - 4	B2	GND	C2	USER I/O - 3
A3	USER I/O - 6	B3	NC	C3	USER I/O - 5
A4	USER I/O - 8	B4	NC	C4	USER I/O - 7
A5	USER I/O - 10	B5	NC	C5	USER I/O - 9
A6	USER I/O - 12	B6	NC	C6	USER I/O - 11
A7	USER I/O - 14	B7	NC	C7	USER I/O - 13
A8	USER I/O - 16	B8	NC	C8	USER I/O - 15
A9	USER I/O - 18	B9	NC	C9	USER I/O - 17
A10	USER I/O - 20	B10	NC	C10	USER I/O - 19
A11	USER I/O - 22	B11	NC	C11	USER I/O - 21
A12	USER I/O - 24	B12	GND	C12	USER I/O - 23
A13	USER I/O - 26	B13	VCC	C13	USER I/O - 25
A14	USER I/O - 28	B14	NC	C14	USER I/O - 27
A15	USER I/O - 30	B15	NC	C15	USER I/O - 29
A16	USER I/O - 32	B16	NC	C16	USER I/O - 31
A17	USER I/O - 34	B17	NC	C17	USER I/O - 33
A18	USER I/O - 36	B18	NC	C18	USER I/O - 35
A19	USER I/O - 38	B19	NC	C19	USER I/O - 37
A20	USER I/O - 40	B20	NC	C20	USER I/O - 39
A21	USER I/O - 42	B21	NC	C21	USER I/O - 41
A22	USER I/O - 44	B22	GND	C22	USER I/O - 43
A23	USER I/O - 46	B23	NC	C23	USER I/O - 45
A24	USER I/O - 48	B24	NC	C24	USER I/O - 47
A25	USER I/O - 50	B25	NC	C25	USER I/O - 49
A26	USER I/O - 52	B26	NC	C26	USER I/O - 51
A27	USER I/O - 54	B27	NC	C27	USER I/O - 53
A28	USER I/O - 56	B28	NC	C28	USER I/O - 55
A29	USER I/O - 58	B29	NC	C29	USER I/O - 57
A30	USER I/O - 60	B30	NC	C30	USER I/O - 59
A31	USER I/O - 62	B31	GND	C31	USER I/O - 61
A32	USER I/O - 64	B32	VCC	C32	USER I/O - 63

VME-P1

Used for +5v,+12v & -12v routing only. IACKIN* tied to IACKOUT*, BGXIN* tied to BGXOUT*.

80pin Interboard Connector 1 Pinout (P5)

This proprietary connector has all the PCI signals along with 4 separate PCI clocks and the 4 request and grants predefined. The CPU board and the Interface boards will be keyed for either 3.3V or 5V signaling. The keying mechanism is based on standoffs. At this point all CPU boards will be 5V PCI signaling. The V/IO pins on the connector are used to define the signaling level to the other PCI boards.

Table 1- 6. Interboard Connector 1 Pinout

Pin	Name	Pin	Name
1	TCLK	41	AD(23)
2	TRST*	42	AD(22)
3	TMS	43	AD(21)
4	TDO	44	AD(20)
5	TDI	45	AD(19)
6	PCI-RSVD9A (Pn2-8)	46	AD(18)
7	PCI-RSVD10B(Pn2-9)	47	AD(17)
8	PCI-RSVD11A(Pn2-10)	48	AD(16)
9	PCI-RSVD14A(Pn1-12)	49	BE2*
10	PCI-RSVD14B(Pn1-10)	50	FRAME*
11	PCI-RSVD19A(Pn2-17)	51	IRDY*
12	PMC-RSVD (Pn2-34)	52	TRDY*
13	PMC-RSVD (Pn2-52)	53	DEVSEL*
14	PMC-RSVD (Pn2-54)	54	STOP*
15	PCICLK3 (NC)	55	PLOCK*
16	PIRQA*	56	PERR*
17	PIRQB*	57	SDONE
18	PIRQC*	58	SBO*
19	PIRQD*	59	SERR*
20	REQ3*	60	PAR
21	PCICLK2 (NC)	61	BE1*
22	REQ1*	62	AD(15)
23	GNT3*	63	AD(14)
24	PCICLK1	64	AD(13)
25	GNT1*	65	AD(12)
26	PCIRST*	66	AD(11)
27	PCICLK0	67	AD(10)
28	GNT0*	68	AD(9)
29	REQ0*	69	AD(8)
30	REQ2*	70	BE0*
31	AD(31)	71	AD(7)
32	AD(30)	72	AD(6)
33	AD(29)	73	AD(5)
34	AD(28)	74	AD(4)
35	AD(27)	75	AD(3)
36	AD(26)	76	AD(2)
37	AD(25)	77	AD(1)
38	AD(24)	78	AD(0)
39	BE3*	79	ACK64*
40	GNT2*	80	REQ64*

Note: This connector supports the V/IO voltage through the center pins. It also supplies power +5V or +3.3V through the center connector for future use. The power for the 956 style adapter will be supplied by that adapter's P1 connector.

80-pin Interboard Connector 2 Pinout (P6)

This connector is a high density proprietary pinout for the AT-bus. In order to keep the connectors for PCI and the AT-bus the same, some signals had to be removed from the interface. The following PC/104 signals are not supported: *MASTER*, 0WS*, DRQ0, DACK0*, DRQ3, DACK3*, DRQ7, & DACK7**. The PC/104 interface will not support master cycles and will only have one 8-bit DMA channel and two 16-bit DMA channels available.

Table 1-7. Interboard Connector 2 Pinout

Pin	Name	Pin	Name
1	SYSCLK	41	SA10
2	OSC	42	SA11
3	SD(15)	43	SA12
4	SD(14)	44	SA13
5	SD(13)	45	SA14
6	SD(12)	46	SA15
7	SD(11)	47	SA16
8	SD(10)	48	SA17
9	SD(9)	49	SA18
10	SD(8)	50	SA19
11	MEMW*	51	BALE
12	MEMR*	52	TC
13	DRQ5	53	DACK2*
14	DACK5*	54	IRQ3
15	DRQ6	55	IRQ4
16	DACK6*	56	SBHE*
17	LA17	57	IRQ5
18	LA18	58	IRQ6
19	LA19	59	IRQ7
20	LA20	60	REF*
21	LA21	61	DRQ1
22	LA22	62	DACK1*
23	LA23	63	RESETDRV
24	IRQ14	64	IOW*
25	IRQ15	65	IOR*
26	IRQ12	66	SMEMW*
27	IRQ11	67	AEN
28	IRQ10	68	SMEMR*
29	IOCS16*	69	IOCHRDY
30	MEMCS16*	70	SD(0)
31	SA0	71	SD(1)
32	SA1	72	SD(2)
33	SA2	73	SD(3)
34	SA3	74	SD(4)
35	SA4	75	SD(5)
36	SA5	76	SD(6)
37	SA6	77	SD(7)
38	SA7	78	DRQ2
39	SA8	79	IRQ9
40	SA9	80	IOCHCK*

Environmental Specifications

Table 1-8. XVME-976 Adapter Module Environmental Specifications

Characteristic	Specification
Temperature Operating Non-operating	 0º to 65ºC (32º to 109.4º F) -40º to 85ºC (-40º to 185º F)
Vibration Frequency Operating Non-operating	 5 to 2000 Hz .015" peak-to-peak displacement, 2.5 g (maximum) acceleration .030" peak-to-peak displacement, 5.0 g (maximum) acceleration
Shock Operating Non-operating	 30 g peak acceleration, 11 msec duration 50 g peak acceleration, 11 msec duration
Humidity	5% to 95% RH, non-condensing

Hardware Specifications

Table 1- 9. Hardware Specifications

Characteristic	Specification
Power Specifications +12V, -12V, +5V	 N/A
Note: Current drawn by the XVME-976 is dependent on the PMC and/or PC/104 modules installed.	

Chapter 2 - SSP Installation

Introduction

The XVME-956/400 SSP is a compact, low power module with two serial ports and a parallel port. The SSP is ideal for embedded applications, where low power consumption, small space, high reliability, and IBM PC or PC/AT software and serial/parallel port compatibility are required.

This chapter describes how to configure and install the SSP Adapter Module. Any or all of the following steps could be involved in a complete configuration and installation:

- Plug in the driver/receiver ICs for the specific option you have chosen for the second serial port.
- Verify and/or adjust the jumper settings.
- Attach cables to the parallel and serial port connectors.
- Install the SSP board to its parent device.

Some operations may not apply to the specific options you have chosen. In such cases, just skip the sections that don't apply, and simply verify that your boards have the proper ICs and jumper settings.

Figure 2-1 shows the locations of the jumper groups and port connectors on the SSP board. Table 2-1 lists the port connectors. Table 2-2 gives an overview of the jumper functions. The jumper groups are numbered W1 - W6 and W11 - W20.

Table 2-1. Port Connector Assignments

Connector	Port
J1	RS-232C serial port COMA
J2	Optional serial port COMB (RS-232C or RS-485)
J3	Parallel port

Table 2-2. Overview of Jumper Functions

Jumper Group	Function
W1 - W3	Port I/O address assignments
W4 - W6	Port interrupt assignments
W11 - W14 W18 - W19	Enable/disable signals from the optional serial port
W15 - W17	Terminators for RS485 lines
W20	Enable/disable bi-directional data on the parallel port

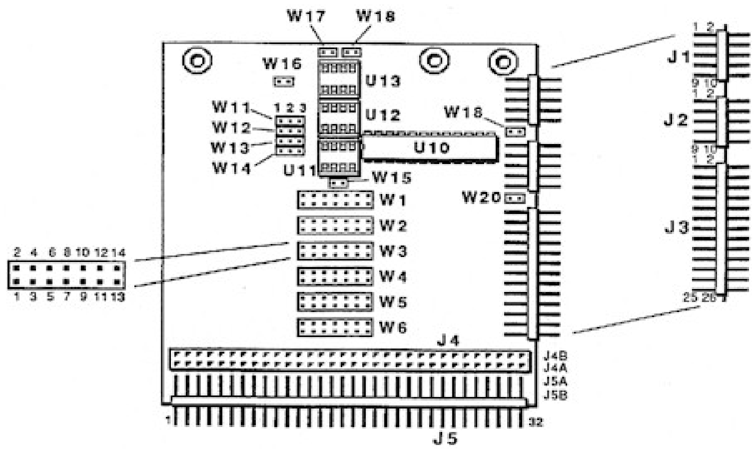

Figure 2-1.Connector and Jumper Locations

Serial Port Driver/Receivers

The serial port COMA is an RS-232C port. The serial port COMB can be configured as an RS-232C or RS-485 port. Implement your selection for this second serial port by plugging in the appropriate driver/receiver ICs, as shown in Table 2-3.

Table 2-3. Serial Port Driver/Receiver ICs

Interface	Driver/Receivers Installed			
	U10 (Max 239)	U11 (75176	U12 (75179	U13 (75179)
RS-232C	in	out	out	out
RS-485 Full Duplex	out	out	in	in
RS-485 Half Duplex	out	in	out	out

Jumper Settings

This section describes how to set the jumpers on the SSP board.

On a 14-pin jumper group, notations such as "1/2" or "7/8" will be used to indicate that you should install a shorting block or wire between pins 1 and 2 or between pins 7 and 8.

On a 3-pin jumper group, the jumper should always be between pins 1 and 2 ("1/2") or between pins 2 and 3 ("2/3").

On a 2-pin jumper group, the jumper will be either present or absent. The notation "short" will indicate that you should install a jumper between pins 1 and 2, while "open" will indicate that you should leave it out.

Base I/O Address Selection

Each port on the board can be assigned a base address at any eight-byte boundary in the PC I/O address space. The address you select, however, must be unique (not the same as that of any other I/O port). For convenient reference, Table 2-4 lists some commonly used I/O port address assignments.

Table 2-4. Common I/O Port Addresses

Port	Base Address (Hex)
LPT1	0378h
LPT2	0278h
COM1	03F8h
COM2	02F8h
COM3	03E8h
COM4	02E8h

Selecting the SSP I/O base address is a two step process. First, choose the appropriate jumper groups via Table 2-5. Second, use Table 2-6 to configure the I/O port address.

Table 2-5. I/O Address Jumper Groups

Connector	Port	Jumper Group
J1	RS-232C serial port COM A	W1
J2	Optional serial port COM B	W2
J3	Parallel port	W3

Within a given jumper group, the individual jumpers set the values of individual I/O base address bits, as shown in Table 2-6. Shorting a particular jumper pin pair sets the corresponding address bit to 0.

Table 2-6. I/O Address Selection Jumper Pins

Pair Shorted	1/2	3/4	5/6	7/8	9/10	11/12	13/4
Bit Cleared	A9	A8	A7	A6	A5	A4	A3

As the table indicates, the jumpers set values for the upper 7 bits of a 10-bit address (since the base address must be on 8-byte boundaries, the last three bits are 0). To determine which jumpers to short, write the three hex characters of the desired address, convert each to binary, ignore the two leading zeros and the last three zeros, and then install jumpers to short the pin pairs corresponding to the remaining zeros in the address.

As an example, suppose that you want to assign base I/O address 02E8h. Converted to binary, this would be 0010 1110 1000. Bits A8 and A4 are zeros, therefore, you would short pin pairs 3/4 and 11/12, leaving all the other pairs open. Usually, the SSP will be used in addition to the XVME PC/AT serial and parallel ports. Hence, Xycom recommends COM A be set to I/O port 03E8, (see Table 2-4), COM B to 02E8 and the parallel port to 0278, (see Table 2-7).

Table 2-7. Xycom Recommended I/O Address Selection

PC/AT Port	**SSP Port**	**I/O Address**	**Pins Shorted**						
			1/2	3/4	5/6	7/8	9/10	11/13	13/14
COM3	COM A	3E8						short	
COM4	COM B	2E8		short				short	
LPT2	Parallel	278		short	short				

Interrupt Selection

Each port can be assigned to an interrupt in the range IRQ2 - IRQ7. Within this range, there are no restrictions on the choice of interrupts, and the interrupt assignments must be unique. Table 2-8 lists some commonly used I/O port interrupts.

Table 2-8. Common I/O Port Interrupts

Port	Interrupt
LPT1	IRQ7
LPT2	IRQ5
COM1	IRQ4
COM2	IRQ3
COM3	
COM4	

Implement your interrupt selections by configuring the appropriate jumper group, according to the table below.

Table 2-9. Interrupt Jumper Groups

Connector	Port	Jumper Group
J1	RS232C serial port COMA	W4
J2	Optional serial port COMB	W5
J3	Parallel port	W6

Within a given jumper group, shorting a particular jumper pin pair assigns a corresponding interrupt, as shown in Table 2-10.

Table 2-10. Interrupt Selection Jumper Pins

Pair Shorted	1/2	¾	5/6	7/8	9/10	11/12	13/14
Interrupt	IRQ2	IRQ3	IRQ4	IRQ5	IRQ6	IRQ7	Pull Down

You are not required to assign an interrupt to a port, however, you will assign interrupts to ports that have incoming data. The parallel port does not usually need to have an interrupt if it is used solely as an output port, such as a printer port. To assign an interrupt to a port, short the corresponding pins on the jumper group for that port. Be sure to short pins 13/14 which will connect a pull-down resistor to the interrupt line.

If COM1 (Port 3F8) or COM2 (Port 2F8) is selected for use on the XVME-956/400, check the BIOS set-up menu on the XVME PC/AT. Type <CTRL><ALT> S to get into set-up. Then disable the internal COM port by setting it to off.

Serial Port Configuration and Connection

The RS-232C port at J2 COMB requires configuration beyond the choice of I/O base address and interrupt described in the previous sections. The serial port at J2 can be configured to operate as a RS-232C or RS-485 port. Jumpers W11 - W14 and W18 - W19 determine the functions of individual interface lines on connector J2. Jumpers W15 - W17 install line terminators. Implement your choice by setting jumpers
W11 - W19, according to Table 2-11.

Table 2- 11. COM B Serial Port Interface Jumper

	W11	W12	W13	W14	W15	W16	W17	W18	W19
RS-232C	2/3	2/3	2/3	2/3	open	open	open	open	short
RS-485 Full Duplex	1/2	2/3	1/2	1/2	open	short	short	short	open
RS-485 Half Duplex	1/2	1/2	1/2	1/2	*	open	open	short	short

*Install short on W15 to terminate RS-485 signal line. RS-485 termination should be installed at the two ends of the line.

Table 2-12. COM B Serial Port Jumper Functions

Jumper			
W11	DSR source selection	2/3 1/2	DSR from RS-232C input Forces DSR active
W12	CTS source selection	2/3 1/2	CTS from RS-232C/RS-485 input Forces CTS active
W14	DCD source selection	2/3 1/2	DCD from RS-232C input Forces DCD active
W15	RS-485 RXD/TXD termination	short open	Terminated (120 ohms) Unterminated
W16	RS-485 RXD termination	short open	Terminated (120 ohms) Unterminated
W17	RS-485 AUXIN termination	short open	Terminated (120 ohms) Unterminated
W18	J2 pin 3	short open	Grounds COM2 pin 3 J2 pin 3 carries RS-232C TXD
W19	J2 pin 5	short open	Grounds COM2 pin 5 J2 pin 5 carries RS-485 AUXIN+

RS-232C Usage - COM A and COM B

Table 2-13 lists the connector pin assignments for the RS-232C port at J1. The entries in this table will also apply to the serial port at J2, if it is configured as an RS-232C port, in accordance with Tables 2-3 and 2-11.

Table 2-13. COM A and COM B Pin Assignments (RS-232C

Signal Name	Function	In/Out	Pin
DCD	Data Carrier Detect	in	1
DSR	Data Set Ready	in	6
RXD	Receive Data	in	3
RTS	Request to Send	out	7
TXD	Transmit Data	out	3
CTS	Clear to Send	in	8
DTR	Data Terminal Ready	out	4
RI	Ring Indicator	in	9
GND	Signal Ground	--	5
EN	(Test use only)	in	--

RS-485 Usage - J2 Full Duplex

Table 2-14 lists the connector pin assignments for the serial port COMB J2. It is configured as full duplex RS-485 port, in accordance with Tables 2-3 and 2-11.

Table 2-14. COM B Pin Assignments Full Duplex (RS-485)

Signal Time	Function	In/Out	Pin
AUXOUT+	Handshake output, high	out	1
AUXOUT-	Handshake output, low	out	6
TXD+	Transmit data, high	out	2
TXD-	Transmit data, low	out	7
GND	Ground	--	3
RXD-	Receive data, low	in	8
RXD+	Receive data, high	in	4
AUXIN-	Handshake input, low	in	9
AUXIN+	Handshake input, high	in	5
----	Not used	--	--

The signal lines shown in Table 2-14, provide for a full duplex operation with handshaking. RS-485 is a differential interface, which provides for greater immunity against noise and interference. This interface will drive cable lengths up to 4000 feet at 57.6K bps. Terminators (120 ohms) are provided for the RS-485 input signals RXD and AUXIN. These terminators are installed by shorting W16 and W17 (refer to Tables 2-11 and 2-12).

The handshake signals usually present on an RS-232C interface (RI, DSR, DCD, CTS, RTS, and DTR) are not fully supported on the RS-485 interface.

Instead, RS-485 uses AUXIN and AUXOUT. For maximum software compatibility, the RS-232C Clear to Send (CTS) handshake input signal for the serial controller is derived from the RS-485 AUXIN signal. Similarly, the RS-485 AUXOUT signal is derived from the RS-232C Request to Send (RTS) handshake output signal from the serial controller. The remaining handshake input signals (RI, DSR, and DCD) are tied active by the jumpers installed at W11, W13, and W14 when this port is configured for RS-485, (refer to Tables 2-11 and 2-12).

If the RS-485 device which you are connecting to this port does not provide an AUXIN signal, then (depending on the software you are running) you may need to loop AUXIN to AUXOUT. Alternatively, you can short W12 pins 1/2 instead or 2/3 to force CTS active.

RS-485 Usage - J2 Half Duplex

Table 2-15 lists the connector pin assignments for the serial port at J2, if it is configured as a half duplex RS485 port, in accordance with Tables 2-3 and 2-11.

Table 2- 15. COMB Pin Assignments Half Duplex (RS-485)

Signal Name	Function	In/Out	Pin
—	Not used	—	1
—	Not used	—	6
TXD/RXD+	Bi-directional data, high	I/O	2
TXD/RXD-	Bi-directional data, low	I/O	7
GND	Ground	—	3
—	Not used	—	8
—	Not used	—	4
—	Not used	—	9
—	Not used	—	5
—	Not used	—	—

The signal lines shown in Table 2-15 provide for half duplex operation. RS-485 is a differential interface, which provides for greater immunity against noise and interference. This interface will drive cable lengths up to 4000 feet at 57.6K bps. Unlike full duplex operation, however, all communication occurs via a single pair of wires. There are no handshaking lines.

RS-485 supports multi-drop operation, that is, more than two devices communicating via a single RS-485 balanced line.

An optional terminator (120 ohms) is provided for the RS-485 TXD/RXD signal. This terminator is installed by shorting W15. However, you should only install this terminator if your board is physically at one end of the line (a 120-ohm terminator should also be installed on whatever device is at the other end of the line).

When the optional serial port is configured for RS-485, the serial controller's Request to Send (RTS) output signal (as set by software) determines the direction (input/output) of the RS-485 driver/receiver. RTS active places the interface in transmit mode, and RTS inactive places the interface in receive mode. It is the responsibility of the user's software to provide a protocol that can handle the bi-directional nature of the interface. The four handshake input signals (RI, CTS, DSR, and DCD) are tied active by the jumpers installed at W11, W12, W13, and W14 when this port is configured for RS-485 (refer to Tables 2-10 and 2-11).

Parallel Port Configuration and Connection

Table 2-16 lists the connector pin assignments for the parallel port at J3. In addition to the pins of connector J3, Table 2-16 also lists the corresponding pins for the DB25F parallel connector cable supplied with the unit. The pinout of J3 is such that it allows the use of a flat ribbon cable between J3 and a PC/AT compatible DB25F parallel connector.

Table 2-16. J3 Pin Assignment

Signal Name	Function	In/Out	J3 Pin	DB25f Pin
-STROBE	Output data strobe	out	1	1
Data 0	Data bit (LSB)	I/O	3	2
Data 1	:	I/O	5	3
Data 2	:	I/O	7	4
Data 3	:	I/O	9	5
Data 4	:	I/O	11	6
Data 5	:	I/O	13	7
Data 6	:	I/O	15	8
Data 7	Data bit (MSB)	I/O	17	9
-ACK	Character accepted	in	19	10
BUSY	Cannot receive data	in	21	11
PAPER EMPTY	Out of paper	in	23	12
SEL OUT	Printer selected	in	25	13
-AUTOFD	Auto feed	out	2	14
-ERROR	Printer error	in	4	15
-INIT	Initialize printer	out	6	16
-SEL IN	Selects printer	out	8	17
-POE	Port output enable	in	26	--
GND	Signal ground	---	10, 12 14, 16 18, 20 22, 24	18-25

Beyond the choice of I/O base address and interrupt described in the previous sections, there is only one jumper that affects the parallel port at J3. This is W20, which controls whether the parallel port will function as a standard PC/AT printer port (output only) or as a bidirectional data port.

The table below shows how to set this jumper.

Table 2-17. Parallel Port Jumper

Parallel Port Usage	W20
PC/AT printer port	short
Bi-directional data port	short

When W20 is open, the direction of data transmission can be controlled by a signal (port output enable) applied to pin 26 of connector J3, or pin 1 of W20. This signal enables data output when low, and data input when high. Only the eight data lines are affected.

A convenient way to generate the port output enable signal is simply to tie J3 pin 26 to one of the parallel port's output control lines (-STROBE, -AUTOFD, -INIT, or -SEL IN). Whichever line you use, be sure that your software controls the line in such a way that you get the data direction you desire.

There are limitations on the total length of cable that can be driven reliably by the ports of the board. A full discussion of these limitations is beyond the scope of this manual. In general terms, the maximum cable length depends on the data rate, and on the amount of noise and interference in the environment. However, you will almost always have reliable data transmission if you observe the following restrictions:

- Parallel Port: Cable length up to 10 feet
- RS-232C Serial Port: Cable length up to 50 feet; data rates up to 19.2K bps
- RS-485 Serial Port: Cable length up to 4000 feet; data rates up to 57.6K bps

Specifications

The table below lists the various operational specifications for the SSP adapter module.

Table 2-18. SSP Specifications

Characteristics	Specifications
Power Requirements	+5V 100mA (+/- 9V for RS232C generated on board)
Temperature	0 - 65º C
Compatibility	Compatible with the XVME-956 expansion scheme and any CPU modules compatible with that scheme.

Chapter 3 SCSI Installation

Introduction

This chapter describes how to install the SCSI Device Controller Module. The SCSI Module provides two software interfaces: the drivers and the BIOS. The drivers are files loaded by the CONFIG.SYS file as devices. They reside in system RAM. The BIOS is an extended BIOS which resides as an 8-bit entity on the AT bus. Either the BIOS or the drivers may be used for system booting. The user must decide which is appropriate for the given application.

The following are mutually exclusive options to be considered in deciding to use BIOS or the drivers:

- Only the BIOS supports booting from the SCSI interface. The drivers cannot be used in these applications
- The drivers' location in system RAM provides faster SCSI interactions
- The BIOS may only be used in systems with one or no standard hard drives. There must be no more than two drives, (standard and SCSI), in the system. The drivers support up to 56 devices and must be used when more than two are needed.
- The BIOS is configured via switches on the module which is typically embedded in the system. The drivers are configured via parameters in the CONFIG.SYS file.
- The BIOS only recognizes SCSI targets 0:0 and 1:0. The drivers must be used to access other targets.
- The BIOS only works with drives. The drivers must be used to access other types of SCSI devices.
- The drivers support multi-tasking. The BIOS does not.
- Removable media hard disks should *only* be installed under the drivers. If installed under the BIOS, *do not change media* or unpredictable results may occur or data may be lost.

Note

Users may boot from one SCSI drive using the BIOS, and then attach other SCSI devices by using the drivers. The drivers will be installed when the config.sys file is run from the first SCSI drive. (See "Booting from a SCSI Drive" section later in this chapter).

Driver Operation

This section describes operation with the module's drivers. Also covered are the utility programs, driver installation, formatting and partitioning of the drives.

Utility Programs

Utility programs were shipped with the module on a diskette. There are two files in the root directory and five in a subdirectory named AFDISK. The following lists the names of these programs:

- Root: ASPI2DOS.SYS
  ASPIDISK.SYS
- AFDISK Subdirectory:
  AFDISK.EXE
  PROGHLP.HLP
  SYS$ERR.DTA
  SYS$MSG.DTA

The two files in the root are the drivers which need to be installed for driver operation. See the Driver Installation section and Partitioning and Formatting section . The five files in the AFDISK subdirectory are used for drive partitioning and formatting (see the API2DOS.SYS section).

Driver Installation

The ASPI2DOS.SYS and ASPIDISK.SYS files need to reside on the boot device. Copy these files, as well as the AFDISK subdirectory files, to that drive. For convenience, you can store these files in a subdirectory.

ASPI2DOS.SYS and ASPIDISK.SYS need to be loaded via the config.sys command file. These drivers require at least twenty buffers and twenty files. This information is defined in the config.sys file as follows:

- buffers=20
- files=20
- device=<path>aspi2dos.sys /z options
- device=<path>aspidisk.sys options

ASPI2DOS.SYS Options

Several non-default options can be specified when installing the aspi2dos.sys driver. These options are specified in the config.sys file on the line which invokes the driver. Command line options may be entered in any order and may be upper or lower case.

Several default values are assumed by the driver. These values may be changed from their default by specifying additional command line options. The default values and their associated command line options are described below:

Default: SCSI disconnect option enabled

- Specify /c to disable this option

Default: SCSI parity option disabled

- Specify /y- to enable this option

Default: SCSI synchronous negotiation option enabled

- Specify /u- to disable this option

Default: SCSI target number 7

- Specify /hx to change this value, where "x" is the desired target number from 0 through 7 inclusive.

Default: AT interrupt level = 11

- Specify /qx to change this value, where "x" is the desired interrupt level and must be one of the following: 09, 10, 11, or 12. The interrupt level switches described, at the end of the chapter, must be set to match the level chosen by this option.

Default: AT I/O address range = 340h-35fh

- Specify /p140 to select I/O range = 140h-15fh. The I/O base address switch, described in Appendix A, must match this selection, even if it is the default value.

Default: Minimal messages displayed during drive installation

- Specify /d to display useful debugging information during installation.

Default: Only LUN=0 will be the address for each SCSI target.

- Specify /1 to cause all LUNs to be addresses when determining which logical units are present on the SCSI bus.

As an example of command line option usage, consider the case where the following options are desired: disconnect enabled, parity enabled, synchronous negotiation enable, SCSI target number = 5, interrupt level = 12, and I/O base address =340h. The following line should appear in config.sys to effect these options:

device=<path>aspi2dos.sys /z /y- /h5 /q12

Aspidisk.Sys

This driver requires the drive to be partitioned by the AFDISK routine prior to driver installation (see Section). If the drive has not been partitioned, the driver will not load and will display an error message.

Aspidisk.sys has two default values:

Default: Minimal messages displayed during drive installation.

- Specify /d to display useful debugging information during installation.

Default: One logical drive will be reserved for removable media devices.

- Specify /rx to reserve additional logical drives. The number representing the number of reserved logical drives is entered in the position indicated by "x". This command line option is ignored if the hard disk is the non-removable type.

Switch Settings

The switch settings need to be considered when using the drivers. Refer to Tables
3-1 and 3-2. Set the following switch options:

- If using the drivers to boot the system, disable the BIOS SW2 positions 1, 2, and 3 all open or all closed.
- Set the I/O base address to the level defined by the command line option.
- Set the interrupt level to that defined by the command line option.
- Enable the hardware interrupts SW2 position 8 open.

The remaining switches have no significance when using the drivers.

Table 3-1. Switch 1 Description

8	7	6	5	4	3	2	1	**SCSI ID**
					O	O	O	7
					O	O	C	6
					O	C	O	5
					O	C	C	4
					C	O	O	3
					C	O	C	2
					C	C	O	1
					C	C	C	0
					O SCSI Parity Enabled C SCSI Parity Disabled			
				OSCSI Sync Negotiations Enabled C SCSI Negotiations Disabled				
			O SCSI Disconnects Enabled C SCSI Disconnects Disabled					
O Diagnostic Messages Disabled C Diagnostic Messages Enabled								

O = Open
C = Closed

Table 3-2. Switch 2 Description

8	7	6	5	4	3	2	1	**BIOS Location**
					O	O	O	Disabled
					O	O	C	DC000
					O	C	O	D8000
					O	C	C	D4000
					C	O	O	D0000
					C	O	C	CC000
					C	C	O	C8000
					C	C	C	Disabled
					O I/O Base Address = 34h			
					C I/O Base Address = 14h			
			O	O Interrupts Level 11				
			O	C Interrupts Level 12				
			C	O Interrupts Level 10				
			C	C Interrupts Level 9				
O Hardware Interrupts Enabled								
C Hardware Interrupts Disabled								

O = Open
C = Closed

Partitioning and Formatting

A utility program named AFDISK is provided to partition and format SCSI drives which are installed under the drivers. Use this utility to:

- Partition SCSI drives into logical disks. Multiple partitions can be created on one physical drive.
- Format SCSI logical drives or partitions.
- Delete existing partitions.

AFDISK provides the functional equivalent of the DOS FORMAT and FDISK utilities. Use AFDISK on drives to be installed under the drivers, *do not use DOS utilities.*

AFDISK Operation

Locate the diskette shipped with the module and copy the five files in the AFDISK subdirectory into a working subdirectory.

To run AFDISK, simply type AFDISK at the DOS prompt. Follow the directions on the screen to partition and format the selected SCSI devices. By pressing the F1 key, the AFDISK utility also provides on-line help.

By pressing the ESC key, the AFDISK utility may be exited at any time without executing any changes.

Reboot the system once the SCSI device(s) are partitioned and formatted. This step saves any changes made and allows use of the newly installed disk(s) or partition(s) by the aspidisk.sys utility.

BIOS Operation

This section describes operation with the module's BIOS, and also discusses module configuration, partitioning, and formatting.

Module Switch Configuration

There are two switch banks on the module which the BIOS reads to configure the SCSI interface, (refer to Tables 3-1, and 3-2). The user will set these switches to affect SCSI options. Each switch bank has eight individual switches which can be opened or closed. Configure these switches as described in the paragraphs that follow.

SCSI Options

All SCSI options must be determined. These options are the following:

- *Module Target Number* - This is a number from 0 to 7 inclusive. This number must be unique and is typically defined as 7 for the module (host).
- *Parity* **-** Parity disabled will not check parity on the SCSI bus. Parity enabled will allow the module to check parity on the SCSI bus. This option is typically enabled.
- *Synchronous Negotiation* **-** When this option is enabled, the module will initiate synchronous negotiations with targets on the SCSI bus. When this option is disabled, the module will not initiate synchronous negotiations, but will respond to negotiations from other targets. This option is disabled for older SCSI targets which do not understand synchronous negotiation protocol. This option is typically enabled.

- *Disconnect* **-** When this option is enabled, SCSI targets are allowed to disconnect from the module if there is a long duration of time for completing the operation requested. They reconnect later when finished. If disconnection occurs, the module will issue INT 15 (busy, wait for disk drive) to allow the host CPU using other software to multi-task. When this option is disabled, the module will not allow targets to disconnect and will not issue any INT 15 calls. This option is typically enabled.
- *I/O Base Address* - This module has 32 registers which require 32 byte locations in the PC/AT I/O space. There are two options: 340H - 35FH or 140H - 15FH. The range chosen must not conflict with other system usage. The range 340 - 35FH is typically chosen.
- *Interrupt Level* **-** This module requires PC/AT interrupt for operation. Levels 9, 10, 11, or 12 may be chosen. The level chosen must not conflict with any other interrupts in the system. Level 10 is typically used by XVME CPU modules and level 9 is typically used by video controllers. Therefore, levels 11 or 12 are good choices.

Diagnostic Messages

If diagnostic messages are enabled, the BIOS will display detailed information during the SCSI connection phase. This lengthens the connection phase as pauses are inserted enabling the user to read the messages. When disabled, no diagnostic information is displayed and the connection phase will be much quicker. This option is usually enabled during initial system debug, then disabled after satisfactory operation has been achieved.

When enabled, the following information will be displayed during connection:

- Adaptec header
- Jumper configuration information
- SCSI device information
- Boot progress report
- Error messages

When disabled, only the Adaptec header and the error messages will be displayed.

Configure the desired diagnostic message option via the switch as described in Section

BIOS Location Address

The BIOS requires 16K bytes in memory. This may be mapped in six locations from C8000H through DFFFFH. Define a location which does not conflict with other system devices.

Hardware Interrupt Enable

The hardware interrupts may be enabled or disabled. There is an incompatibility among the module's BIOS, DOS 4.0.1, and some CPU's BIOS. This incompatibility causes the system to stop running during a SCSI boot operation. However, this is not a problem when the SCSI drive is not the boot device or when a DOS version other than 4.0.1 is being used. In situations where DOS 4.0.1 has to be used and the SCSI drive has to be the boot device, interrupts may be disabled and the system will boot correctly.

BIOS Functionality

The BIOS will only support SCSI disk drives and will support a maximum of two drives. The BIOS only recognizes target:LUN values of 0:0 and 1:0. If there is one SCSI drive, assign its target number to 0:0. If there are two SCSI drives, assign their target numbers to 0:0 and 1:0. The BIOS will not recognize any drives with target numbers 2:0 and higher.

If there are two standard drives, the BIOS will not connect any SCSI drives. However, if there is one standard drive, a maximum of one SCSI drive will be connected by the BIOS. If there are no standard drives, the BIOS will connect a maximum of two SCSI drives. Use the drivers to overcome these limitations.

The BIOS will assign SCSI drives sequentially after the standard hard drive. That is, if there is one standard drive and a SCSI drive, the standard drive will be assigned to C: and the SCSI drive (0:0) will be assigned to D:. If there are no standard drives and one SCSI drive, the SCSI drive (0:0) will be assigned to C:. If there are no standard drives and two SCSI drives, the SCSI drive (0:0) will be assigned to C: and the SCSI drive (1:0) will be assigned to D:.

BIOS Booting Contentions

When a SCSI drive is assigned to C: and there is no floppy diskette installed in A:, the BIOS will attempt to boot from the SCSI drive 0:0 assigned to C:. If there is a diskette in A:, the system BIOS will attempt to boot from A:.

If a standard drive is assigned to C:, then the system BIOS will attempt to boot from the standard drive and no attempt will be made to boot from the SCSI drive.

Partitioning and Formatting

The DOS FDISK program is used to partition drives installed under the BIOS. The DOS FORMAT program is used to format drives installed under the BIOS. Use the /S option of the format program if the SCSI drive is to be the boot device. Do not use the AFDISK utility provided with the drivers, this is for driver usage only.

If the drive was previously partitioned with a utility other than FDISK, it may be necessary to delete the partitions with that utility before repartitioning the drive with FDISK. This is true for the driver utility AFDISK as well. Failure to observe this can prevent a SCSI drive from booting properly, even though it appears to be configured correctly.

Booting from a SCSI Drive and Installing Drivers on that Device

1. To create a system which boots from a SCSI drive yet also allows removable media or three drives in the system, perform the following steps:
2. Boot from the first SCSI drive following directions in Section, BIOS Operation.
3. Install the software drivers as outlined in Section, Driver Operation.
4. Ensure that the target number of the SCSI device to be installed under drivers is greater than 1:0, i.e. with the SCSI drives: the boot SCSI drive should be 0:0 and the drive to be installed under drivers should b 2:0. This usually requires a jumper configuration on the second SCSI drive.
5. Ensure SW2 positions 1, 2, and 3 are set to the desired BIOS address.
6. Ensure all driver parameters agree with the switch settings.

Cable Installation

The SCSI devices communicate through the SCSI bus which is a 50 pin flat cable. There will be between two and eight devices on the bus.

Pin one needs to be oriented properly on each SCSI device. A 50 pin connector is provided through the module's front panel. Pin one is located at the top of the connector when the module is mounted into a VMEbus system. Check the manuals for the proper orientation of pin one on the other SCSI devices connected to the bus.

The two SCSI devices at each end of the bus need to have terminating resistors installed for proper operation. All other SCSI devices must have their terminators removed. The module provides optional termination, in the form of three sip sockets, with terminating sip resistors installed at the factory. These are RN3, 4, and 5. Remove these resistor networks if the module is not on an end of the SCSI cable.

Another consideration is that of target number assignment. Each device on the SCSI bus needs to have a unique target number (ID) assigned.

Connector Definition

The SCSI bus connector utilizes a 50 pin connector which is available through the front panel. The pin definition of this connector is listed in Table 3-3.

Table 3-3. Pin Definitions

SIGNAL NAME	PIN
DATAO*	2
DATA1*	4
DATA2*	6
DATA3*	8
DATA4*	10
DATA5*	12
DATA6*	14
DATA7*	16
PARITY	18
GND	20
GND	22
GND	24
TERM POWER (FUSED)	26
GND	28
GND	30
ATN*	32
GND	34
BSY*	36
ACK*	38
RST*	40
MSG*	42
SEL*	44
C/D*	46
REQ*	48
I/O*	50

Note

Pin 25 is open. All remaining odd pins are grounded.

Specifications

Table 3-4 lists the various operational specifications for the SCSI adapter module.

Table 3- 4. Specifications

Characteristics	
PowerRequirements	+5V 0.43 A, typical 0.63 A, maximum
Temperature	0-65ºC
Compatibility	Compatible with XVME-956 expansion scheme and any CPU modules compatible with that scheme.

Chapter 4 - Memory Expansion Module Installation

Memory Expansion Module Installation

The XVME-956/101 Memory Expansion Module (MEM) is an embedded system module which provides a convenient means to expand your Xycom VME AT system. The XVME-956/101 MEM four byte-wide memory sockets are organized into two groups of two sockets each. Each group can be configured for a different type of memory device, allowing many possible memory configurations. All of the 32 to 512 Kbyte static RAMs, as well as many types of Flash EPROMs are supported.

This chapter describes how to configure and install the memory expansion module. Before using the memory expansion module, install the memory devices and verify the jumper settings.

Jumper Configuration Summary

Table 4-1 summarizes the expansion module unit's configuration jumpers.

Table 4-1. Jumper Option Summary

Jumper	Function
W1	Write enable/protect for devices in sockets A and B
W2	Jumpering for Sockets A and B
W3	Jumpering for Sockets A and B
W4	Jumpering for Sockets A and B
W5	Interrupt Level Selection
W6	Write enable/protect for devices in sockets E and F
W7	Jumpering for Sockets E and F
W8	Jumpering for Sockets E and F
W9	Jumpering for Sockets E and F
W10	Power fail trip point
W11	Board number, I/O port, Memory window address
J2	Reserved
J3	Flash EPROM programming enable
J4	External backup battery #1 connector
J5	External backup battery #2 connector

**For information regarding the use of the XVME-956/101 as a Solid State Disk, please refer to the XVME-971 package and manual.*

The figure below shows the location of the module's sockets, jumpers, and other features.

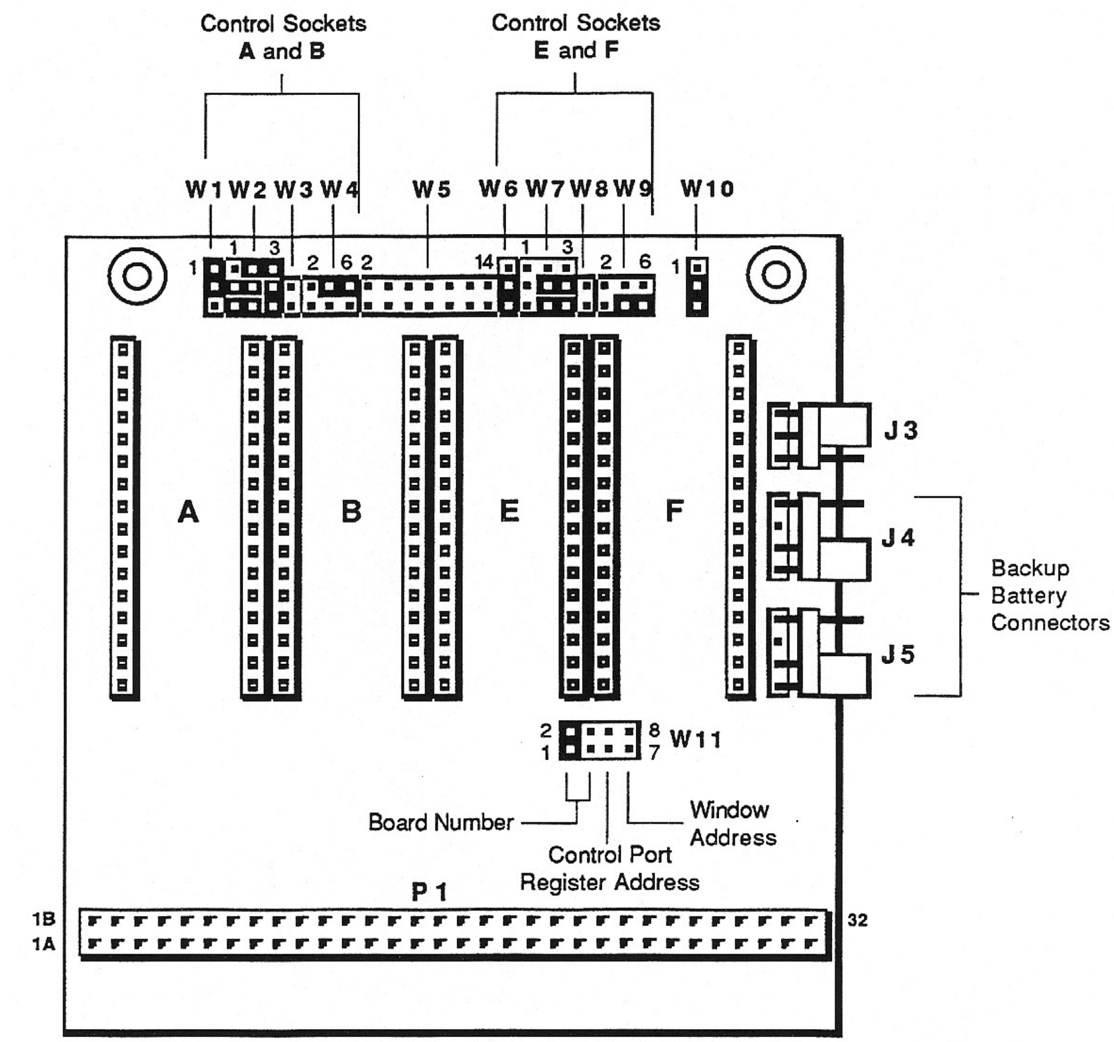

Figure 4-1. Connector and Jumper Locations

General Module Setup

This section describes how to configure the following:

- Window Address
- System Power Fail Interrupt
- Control Register Address
- Board Number

Note

The jumper tables use the convention "/" to mean the two pins shorted. This means that "3/4", (pins 3 and 4), of the jumper array are connected with a shorting block.

Window Address Selection

The expansion memory appears in a 64K window at address D0000H or E0000H. The XVME PC/AT CPUs use the E0000H block for VMEbus Real Mode Window accesses. If code on the memory expansion module will require use of the VMEbus Real Mode Window, the memory expansion module must reside at D0000H. The expansion module requires the use of the entire D0000H segment of 64 Kbytes. If another PC/AT device resides anywhere within this 64K block, e.g. at D0000H, contention will occur if W11 7/8 is open. If W11 7/8 is shorted, selecting E0000H, the code on the memory expansion module, cannot access the VMEbus through the Real Mode Window. This is because the Real Mode Window resides at E0000H.

Table 4-2. Window Address Selection (W11)

Jumper	Function
W11 7/8 open*	Selects window address D0000h
W11 7/8 shorted	Selects window address E0000h
*Default	

Control Register Port Address

The MEM unit has two control registers called Control Register 1 and Control Register 2. These are I/O mapped, 8-bit registers.

Register 1 selects:

- Module by board number
- Socket (A, B, E, or F)
- Which portion of a large device will appear in the window

Register 2 controls:

- Two bits for selecting pages in large devices
- Device write enable
- Flash EPROM (+12) volt programming voltage enable
- Battery voltage and system power fail flags

The registers are accessed by writing to the Control Register Port Address, selected by W11pins 5 and 6. Port address selection is shown in Table 4-3.

Table 4-3. *I/O Port Address Selection (W11)*

Jumper	Function
5/6 Open*	Control Register 1 I/O address 274h, Control Register 2 I/O Address 674h
5/6 Shorted	Control Register 1 I/O address 275h, Control Register 2 I/O Address 675h
*Default	

Board Number (W11)

Each memory expansion module is identified by a "Board Number" from 0 to 3. A unique Board Number allows up to four expansion modules to reside at a single I/O Port Address without bus conflicts. The Board Number is set by jumpering W11as shown in Table 4-4. Practical considerations limit the number of expansion modules in a system to six. There can be multiple modules with Board Numbers 1, 2, or 3 as long as they are at different port addresses. However, only one module in the entire system may be Board Number 0.

Table 4-4. Board Number Selection

Board Number	Short
Board number 0	1/2, 3/4
Board number 1*	1/2
Board number 2	3/4
Board number 3	none
*Default	

Upon power-up or reset, the module jumpered as board number 0 (both jumpers on) is enabled, allowing the ROM-BIOS or an application program to detect active memory at that address. For instance, at power-up time, the ROM-BIOS will scan D0000h for a distinctive bit pattern, (55AAh) and, if found, execute the program at that address.

Power Fail Interrupt Jumpers (W10, W5)

When the +5V system, (not battery), voltage falls below a trip point (selected by W10) of either 4.75V or 4.5V, on-board circuitry generates a power fail signal. Table 5-5 shows which jumper pins to short at W10 to select the trip level.

Jumpers at W5 select which interrupt (if any) to generate when a power fail signal is received. The power fail interrupt signal can be connected to any of the IRQ lines on the PC bus or to the -IOCHCK line, which is a non-maskable interrupt (NMI). Table 4-6 shows which pins to short to select a particular interrupt. The power fail signal remains active until the voltage level returns to a normal value (above the trip level).

Note

Remember that the XVME PC/AT will reset when the VMEbus power dips to 4.85. However, the memory expansion module power fail interrupt circuitry should not be relied upon for system shut down notice.

Table 4- 5. Power Fail Interrupt Trip Level (W10)

Jumper	Function
2/3*	Sets trip point at 4.25V to 4.50V
1/2	Sets trip point at 4.50V to 4.75V
*Default	

Table 4-6. Power Fail Interrupt Selection (W5)

Pins	Interrupt
12/14*	IOCHK (NMI)
1/2	IRQ7
3/4	IRQ6
5/6	IRQ5
7/8	IRQ4
9/10	IRQ3
11/12*	Pull-Down
*Do Not Connect 11/12 if IOCHK is Selected	

Memory Device Configuration (W1-4, W6-9)

The memory expansion module's four sockets are organized as two groups of two sockets each. Configuration for various devices to be used in each group is controlled by jumper arrays W1-4 for sockets A and B, and W6-9 for sockets E and F.

Each group of sockets must contain devices of a single type. Different groups of sockets can have different devices. For example, Group 1 (sockets A and B) could both be EPROMs, and group 2 (sockets E and F) could both be SRAMs. However, you cannot use a SRAM in socket A, and an EPROM in socket B.

Jumper arrays W1-4, and W6-9, are each associated with an array of pins as shown in Figure 4-2.

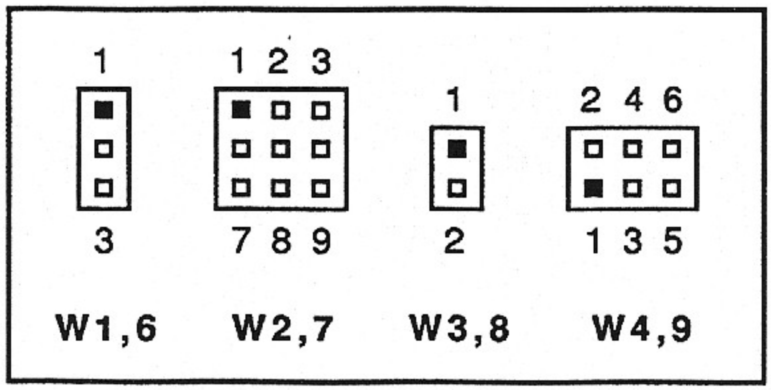

Figure 4- 2. Byte-Wide Socket Configuration Jumpering (W1-4 and W6-9)

Caution

When changing the jumper blocks on a jumper array, be sure to remove any jumper blocks that may be on the jumper array if they are not specified in the table.

Installing 28-Pin Devices in 32-Pin Sockets

Figure 4-3 displays 28-pin devices in 32-pin sockets. Pins 1, 2, 31, and 32 are unused, (socket pin 3 becomes pin 1 of the 28-pin device, socket pin 30 becomes device pin 28 etc.).

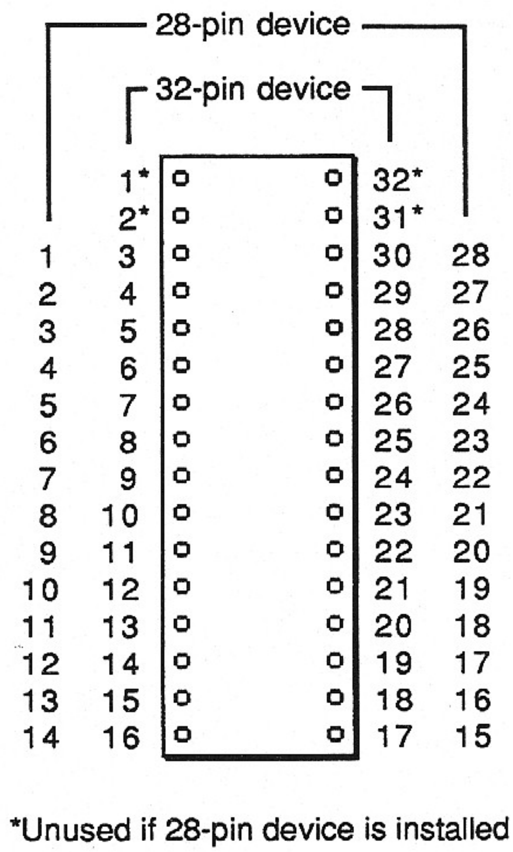

Figure 4- 3. 28-Pin Device in a 32-Pin Socket

Static RAM Jumpering

To install Static RAMs (SRAMS), jumper the byte-wide sockets according to the contents of Table 4-7, and then plug in the devices. Connect the off board battery to provide back-up power to the SRAMs. See the Battery Backup Configuration section in this chapter for details of battery connections.

Table 4-7. SRAM Jumpering

Name	Size	Mfgr.*	Pins	Jumpering			
				W1, 6	W2, 7	W3, 8	W4, 9
µPD43256A	32K	NRC	28	**	5/6, 8/9	Open	3/5, +
MSM51257(L)RS	32K	OKI	28	**	5/6, 8/9	Open	3/5, +
TC55257AP(L)	32K	Toshiba	28	**	5/6, 8/9	Open	3/5, +
HM62256	32K	Hitachi	28	**	5/6, 8/9	Open	3/5, +
HM628128	128K	Hitachi	32	**	4/7, 5/6, 8/9	Open	3/5, +
HM628512	512K	Hitachi	32	**	1/2, 4/7, 5/6, 8/9	Open	1/8, +

Notes
* or equivalent
** 1/2 for software controlled write enable; 2/3 for writing always enabled
\+ 2/4 connects back-up battery; 4/6 if back-up battery is not desired

To install NOVRAM devices, jumper the byte-wide sockets according to the contents of Table 4-8, then plug in the devices. NOVRAM devices contain batteries, therefore, off-board batteries are not required.

Table 4-8. NOVRAM Jumpering

Name	Size	Mfgr.*	Pins	Jumpering			
				W1, 6	W2, 7	W3, 8	W4, 9
DS1235Y	32K	Dallas	28	**	5/6, 8/9	Open	3/5, 4/6
DS1245Y	128K	Dallas	32	**	5/6, 8/9, 4/7	Open	3/5, 4/6

Notes
* or equivalent
** 1/2 for software controlled write enable; 2/3 for writing always enabled

EPROM Jumpering

To install EPROMs, you must first program the EPROMs with an EPROM programming device. Once the EPROMS are programmed, jumper the sockets according to the contents of Table 4-9, then plug in the devices.

Table 4- 9. EPROM Jumpering

Name	Size	Mfgr.*	Pins	Jumpering			
				W1, 6	W2, 7	W3, 8	W4, 9
27(C)256	32K	ALL	28	–	6/9	Open	3/5, 4/6
27(C)512	64K	ALL	28	–	6/9, 7/8	Open	3/5, 4/6
µPD27C1001A	128K	NEC+	32	1/2	2/3, 4/5, 6/9, 7/8	Open	5/6
HN27C101	128K	Hitachi	32	1/2	2/3, 4/5, 6/9, 7/8	Open	5/6
TC571000D	128K	Toshiba	32	1/2	2/3, 4/5, 6/9, 7/8	Open	5/6
MSM271000AS	128K	OKI	32	1/2	2/3, 4/5, 6/9, 7/8	Open	5/6
27010	128K	Intel	32	1/2	2/3, 4/5, 6/9, 7/8	Open	5/6
27020	256K	Intel	32	1/2	2/3, 4/5, 6/9, 7/8	Open	1/3, 5/6
µPD27C2001	256K	NEC+	32	1/2	2/3, 4/5, 6/9, 7/8	Open	1/3, 5/6
27040	512K	Intel	32	1/2	1/4, 2/3, 6/9, 7/8	Open	1/3, 5/6
27513**	64KP	Intel	28	1/2	5/6	Open	3/5, 4/6
27011**	128KP	Intel	28	1/2	5/6	Open	3/5, 4/6

Notes

* or equivalent (certain NEC EPROMs cannot coexist on the same module with battery backed RAM because they draw significant backup battery current through their chip select inputs and may cause battery failure)

** Page-address EPROMS

Restrictions on EPROM Use

NEC EPROMs 27C1001, and 27C1002 cannot coexist on the same module with battery backed RAM. These EPROMs draw significant current (> 1mA) through their Chip Select inputs and may cause failure of the back-up battery. Signetics 27C256 may draw up to 10 uA through its Chip Select inputs when not powered. Though substantially less than the NEC part, it is still much greater than the usage (typically < 1 uA) by other devices. Use of such devices may limit battery life. It is your responsibility to determine the proper devices for your application.

Flash EPROM Jumpering

To install Flash EPROMs, jumper the byte-wide sockets according to the contents of Table 4-10, then plug in the devices.

Table 4-10. Flash EPROM Jumpering

Name	Size Bytes	Mfgr.*	Pins	Jumpering			
				W1, 6	W2, 7	W3, 8	W4, 9
28C256	32K	Atmel	28	1/2	5/6, 8/9	Open	3/5, 4/6
29C256	32K	Atmel	28	1/2	5/6, 6/9	Open	3/5, 4/6
28F256	32K	Intel	28	1/2	2/3, 4/5, 6/9	Open	4/6
28F512	64K	Intel	28	1/2	2/3, 4/5, 6/9, 7/8	Open	4/6
28F010	128K	AMD	32	1/2	2/3, 4/5, 5/9, 7/8	Open	4/6
28F020	256K	Intel	32	1/2	2/3, 4/5, 6/9, 7/8	Open	1/3, 4/6
* or equivalent							

Flash EPROM Programming Voltage

If 5 volt Flash EPROMs are used, you can connect the programming voltage by jumpering W2 or W7 as indicated in Table 4-11. The programming voltage is then gated to the device with software, as part of the programming algorithm.

Table 4-11. EPROM Programming Voltage

Program Voltage	Jumpering			
	W1, 6	W2, 7	W3, 8	W4, 9
5V	1/2	5/6, 8/9	Open	3/5, 4/6
5V	1/2	5/6, 6/9	Open	3/5, 4/6
12V	1/2	2/3, 4/5, 6/9	Open	4/6
12V	1/2	2/3, 4/5, 6/9, 7/8	Open	4/6
12V	1/2	2/3, 4/5, 5/9, 7/8	Open	4/6
12V	1/2	2/3, 4/5, 6/9, 7/8	Open	1/3, 4/6

If 12 volt Flash EPROMs are used, you will have to supply the 12 volt programming voltage while programming the devices. This can come from the PC bus, or an external power supply. To use the PC bus voltage, connect J3, pins 1 and 2. To use an external power supply, connect the 12 volts to J3, pin 2, with the return to J3, pin 3. After programming the devices, you can remove the 12 volt supply, or the jumper from J3 1/2. Table 4-12 shows a summary of connector J3.

Table 4-12. Connector (J3)

Function	Pin
From PC bus +12 volts	1
To Vpp (W2 and W7, pin 3)	2
Ground	3
Default is 1/2	

Jumper Array Summary

Tables 4-13 through 4-16 show a summary of the functions for each pin of each jumper array (W1-4; W6-9). These tables give information on jumpering a socket group for devices not found in the jumpering tables, and also, which signal appears on each jumper pin and what pins they can connect to on the 32-pin sockets.

Note

In Tables 4-13 through 4-16, "From" indicates the source of the signal, and "To" indicates the destination of a particular line.

Table 4-13. Summary of Jumper Array (W1, W6)

Function	Pin
From write strobe (gated)	1
To (W2 or W7) pin 5	2
From write strobe (ungated)	3

Table 4-14. Summary of Jumper Array (W2, W7)

Function	Pin
From address bit A18 (PS2)	1
To socket pin 1 and W3/W8 pin 2	2
Flash EPROM programming +12V	3
To socket pin 31	4
From write protect option	5
To socket pin 29	6
From address bit SA15	7
To socket pin 3	8
From address bit SA14	9

Table 4- 15. Summary of Jumper Array (W3, W8)

Function	Pin
From SA19 (PS3)	1
To socket pin 1 and W2/W7 pin 2	2

Table 4- 16. Summary of Jumper Array (W4, W9)

Function	Pin
From address bit A17 (PS1)	1
From back-up battery power	2
To socket pin 30	3
From socket pin 32	4
From socket pin 32	5
From Vcc	6

Battery Backup Configuration And Battery Information

This section covers how to connect external backup batteries to protect the contents of SRAMs. It also discusses important safety aspects of using lithium batteries.

Safety Information

Note

Lithium batteries may explode if mistreated. Please observe the following important safety precautions:

- ***Do not recharge, disassemble, heat above 100 C (212 F), or dispose of in fire.***
- ***Dispose of used batteries promptly. KEEP AWAY FROM CHILDREN.***
- ***External batteries MUST NOT exceed 4.0 V or damage to the module may result.***
- ***Observe correct polarity when installing the backup battery. Reversed polarity can damage the module, and can cause the battery to explode.***

Battery Connection

One battery will protect the contents of SRAM memory. A second battery will provide additional security as on-board circuitry automatically selects the battery with the highest voltage as the source for backup current. External batteries are connected at J4 (BAT1) and J5 (BAT2). Table 4-17 summarizes the function of each pin in connectors J4 and J5. If SRAMs on the module unit are to be made non-volatile with the batteries.

Table 4- 17. Backup Battery Connectors (J4 and J5)

Pin	Function
J4-1	Backup Battery 1 (3.6 VDC)
J4-2	Key (no connection
J4-3	Backup Battery 1 (3.6 VDC)
J4-4	Ground
J5-1	Backup Battery 1 (3.6 VDC)
J5-2	Key (no connection)
J5-3	Backup Battery 1 (3.6 VDC)
J5-4	Ground

Battery Replacement

To maintain backup current to the devices, a good battery must be connected to J4 or J5 at all times. You can change one battery at a time. Figure 4-4 shows the J4 connector. (See Figure 4-1 for the location of the J5 connector). If only one battery is connected, remove the short from the unused battery connector and connect a new battery. Then remove the old battery, and short pins 3/4 of the connector or connect a second battery. If two good batteries are connected, you can remove either, and the other will protect memory contents as long as it has sufficient voltage.

Installation to Carrier Card

For proper installation, refer to Chapter One for Type B module assembly to the XVME-976.

XVME-976 Installation

Figure 4-4 shows the front panel assembly of the XVME-976 memory expansion module.

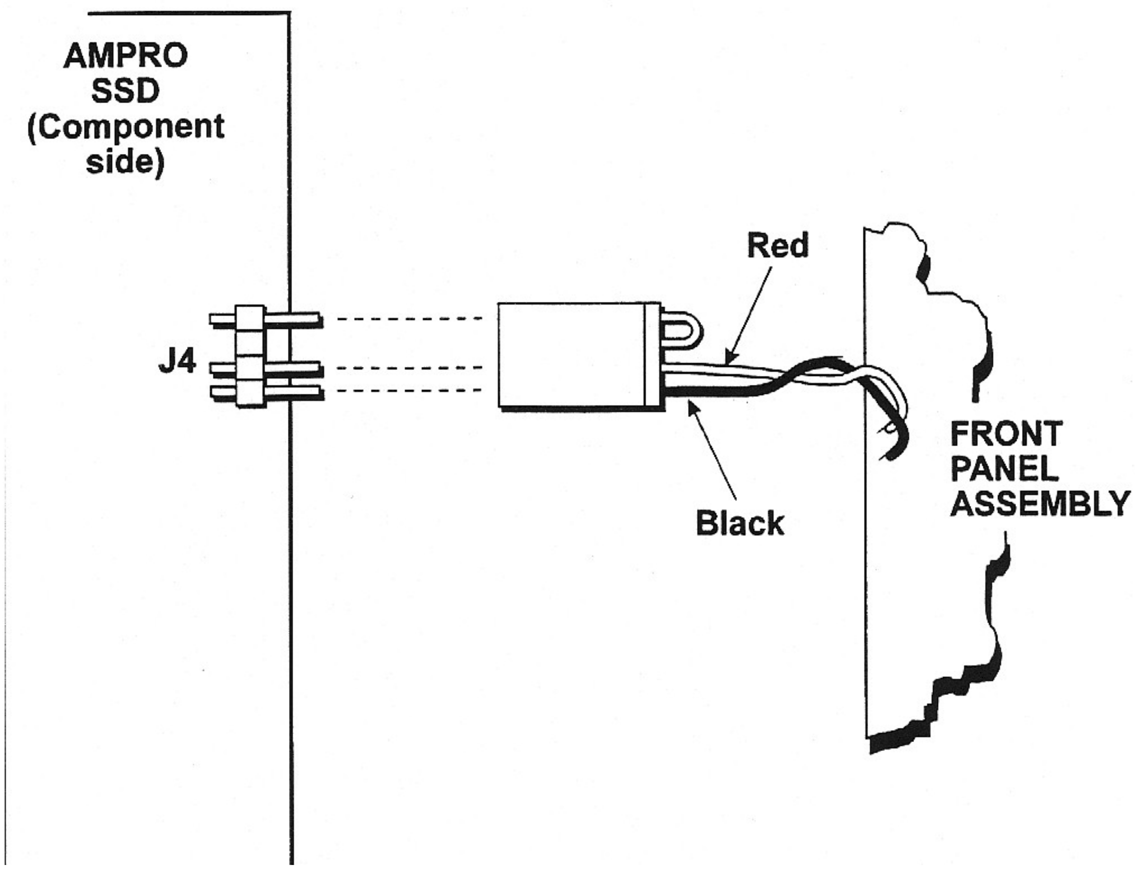

Figure 4- 4. XVME-976 Memory Expansion Module Front Panel Assembly

Installing the XVME-956/101

The XVME-956/101 is shipped with a special mylar insulator that protects the battery connections. The installation of the XVME-956/101 is similar to that of a Type B, which is explained in Section 1.3.4, with the exception of the mylar insulator. Follow these steps to secure the XVME-956/101 mylar insulator.

1. Secure the XVME-956/101 mylar insulator using nylon screws at position 4 (shown in Figure 4-5).
2. Place the XVME-956/101 module on the XVME-976 making sure the pins on the XVME-976 are aligned with the sockets on the XVME-956/101.
3. Connect the battery cable from the front panel to the appropriate connector on the XVME-956/101. Next, secure the front panel to the XVME-976 using the two screws labeled 2 in Figure 4-5.
4. Fold the mylar insulator back over the XVME-956/101 and secure it to the XVME-956/101with the screws labeled 3 in Figure 4-5.
5. Secure the mylar insulator and front panel battery assembly using screws labeled 1 in Figure 4-5.

Figure 4-5 shows the mylar insulator and front panel assembly of the XVME-956/101 memory expansion module.

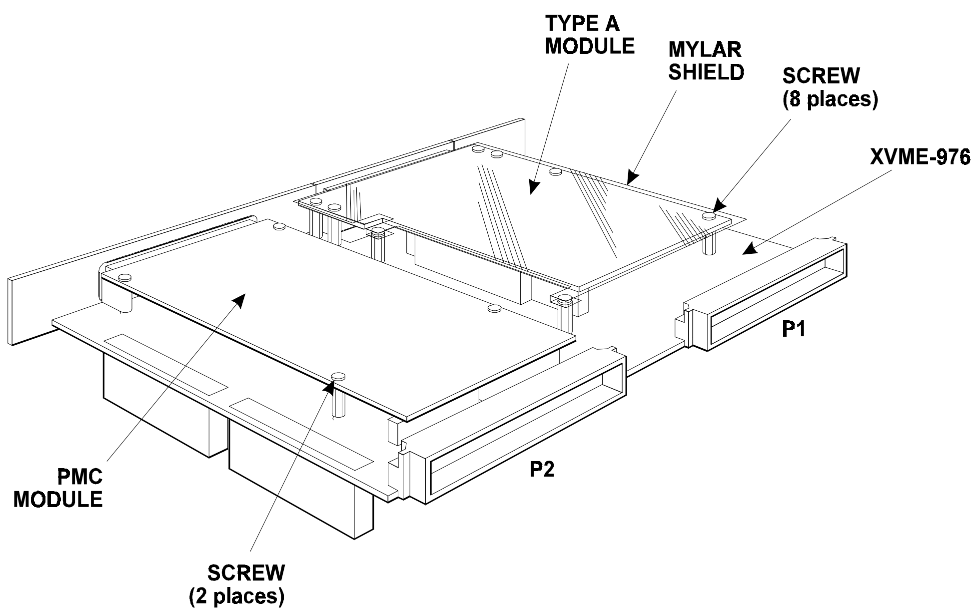

Figure 4-5. XVME-956/101 Type A Module

Programming

This section presents reference information to help you understand the XVME-956/101 unit programming interface. It also provides information on control register functions and how to read the registers for power alarm, and battery voltage monitoring. Data is also included on selecting pages within large memory devices, board number, window address, and Flash EPROM programming.

Control Register Usage

The control registers are I/O mapped, 8-bit registers that enable certain functions and provide information about others. These functions are discussed in detail in the sections following.

In systems with multiple XVME-956/101 modules, all modules at the same I/O port address receive the same information in their control registers. However, because Board Number is decoded from the contents of Control Register 1, only one module per address is selected. At **power up** and **CTRL-ALT-DEL reset**, the control registers are reset to all zeros by the BIOS.

Control Register 1 Functions

The contents of Control Register 1 selects a particular XVME-956/101 module by board number, selects a particular socket on that module, and selects "pages" of large devices in that socket.

To select a particular socket, write the lower 3 bits of control register with the desired socket number (in binary). The binary addresses of the sockets are given in Table 4-18.

Table 4-18. Socket Selection

Socket	Number Bit: 3 2 1
A	0 0 0
B	0 0 1
E	1 0 0
F	1 0 1

Table 4-19 shows the Control Register 1 bit usage.

Table 4- 19. Control Register 1 Bit Usage

	Board		**Page Select**		**Res***	**Socket Numbers**		
Bit	7	6	5	4	3	2	1	0
Name	BD1	BD0	PS1	PS0	*	SN2	SN1	SN0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Description								
Bits 7, 6 (BD0, BD1)	Board Number. Module is selected if these bits match board number jumpering of W11 pins 1-4.							
Bits 5, 4 (PS0, PST)	Page Select. Used to select 64K byte pages from larger memory devices. PS2 and PS3 are in Control Register 2.							
Bit 3	*Reserved							
Bits 2-0 (SN0-SN2)	Socket number in binary where SN0 is the LSB.							

Control Register 2 Functions

The content of Control Register 2 provides additional device page selection information, +12 volt Flash EPROM programming voltage control, SRAM write protect, power fail alarm monitoring, and battery voltage monitoring. Table 4-20 indicates the use of the various register bits.

Table 4- 20. Control Register 2 Bit Usage

	Power			**Address**	**Write Enable**	**Flash**	**Address**	
Bit	7	6	5	4	3	2	1	0
Name	VB2	VB1	-PFIRQ	-	-WEN	VPP	PS3	PS2
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W
Description								
Bits 7, 6 (VB1-2)	Battery monitor. 1= dead or missing battery. Bit 6 = battery 1 (J4), Bit 7 = battery 2 (J5).							
Bits 5 (-PFIRQ)	Power fail interrupt status. Zero if system (*not battery*) power falls below threshold.							
Bit 4	Ampro reserved. Always set to 0.							
Bit 3 (WEN)	Software controlled write protect for SRAMs or Flash EPROMs. 1 is write protect, 0 is enabled,							
Bit 2 (VPP)	12 volt Flash EPROM programming voltage. Enabled (=1) by software.							
Bits 0-1 (PS2, PS3)	Page select. Used to select 64K byte pages from larger memory devices. PS1 and PS2 are in Control Register 1. (See Table 3-2.)							

The following is some additional information on the usage of Control Register 2.

- Read only bits 7 and 6 indicate battery voltage. If the bit is a zero, the battery is above the threshold (2.2 VDC). A one indicates the battery is below the threshold (<2.2 Vdc) or not installed. Bit 7 is VB2, the battery connected to J5. Bit 6 is VB1, the battery connected to J4.
- Bit 5 is the power fail alarm. A zero means system (*not battery*) voltage has dropped below the voltage selected with W10.
- Bit 4 is reserved. Always set this bit to zero when writing to register 2 (674h or 675h).
- Bit 3 (-WEN0) provides a software controlled write protect/write enable bit. It allows write protection of SRAMs and Flash EPROMs. If bit 3 is zero, the PC bus signal -SMEMW is available to the byte-wide sockets, allowing normal read/write operation. If bit 3 is a one, writing to devices in the byte-wide sockets is inhibited. With writing inhibited, these become read-only devices.
- Bit 2 provides software control of the +12 Vpp for Flash EPROM programming. Flash EPROM programming is discussed later in this chapter. If this bit is one, +12 volts is routed to W2-3 and W7-3.
- Bits 1 and 0 are used to select 64K byte pages of larger memory devices. (See Figure 4-5.)

Reading the Registers

Both Control Registers are readable. Control Register 1 and most of 2 are writable. Three read-only bits (7-5) in Control Register 2 provide information about the state of the off board batteries and the power fail alarm.

Reading Control Register 2 is the same. Control Register 2 is located at 674h or 675h, but its output is controlled by the board number select logic. To read Control Register 2 of Board Number 1 at address 674h, write to register 1, at 274h, specifying Board Number 1. This will enable the output of *only* Register 2 of that module to be read (at address 674h). To check the status of the backup batteries on that module, read bits 6 and 7. The following example is a simple assembly language routine that accesses these bits:

Table 4- 21. Assembly Language Routine Example

MOV	AL, 40h	;	Board Number 1
MOV	DX, 274h	;	Port Address 274h
OUT	DX, AL	;	Outputs Board Number to Control Port Address
MOV	DX, 674h	;	Selects Control Register 2 as source of data
IN	AL, DX	;	Inputs data from Control register 2
AND	AL, 11oooooob	;	Masks all but Battery Monitor bits
		;	Returns will not be Zero if a battery is low
RET			Return

Selecting Portions of Large Devices

The memory window is 64 Kbytes in size. If the memory devices are the same size as the window, their entire contents appear in the window when that device is selected. If the device is smaller than the window, its contents are mirrored in the window. For example, a 32 Kbyte memory will appear twice in a 64 Kbyte window, once at D0000h, and again at E0000h.

If the memory device is larger than the window, only part of its contents can appear in the window. The part of the device to appear is selected via the PS0-3 bits in the control registers. These bits are used as high order address lines, A16 through A19, by the memory devices. They are set by writing to the control registers with I/O instructions.

A 128 Kbyte device can appear as two 64 Kbyte "pages" so only PS0 is required to select the upper

(PS0 = 1) or lower 64K (PS0 = 0) 64 Kbytes. All four bits select up to 16 (64 Kbyte) pages of a 1 Mbyte memory. Figure 4-6 shows a 64 Kbyte portion of a 1 Mbyte memory being selected. PS0 is the LSB (A16), and PS3 is the MSB (A19).

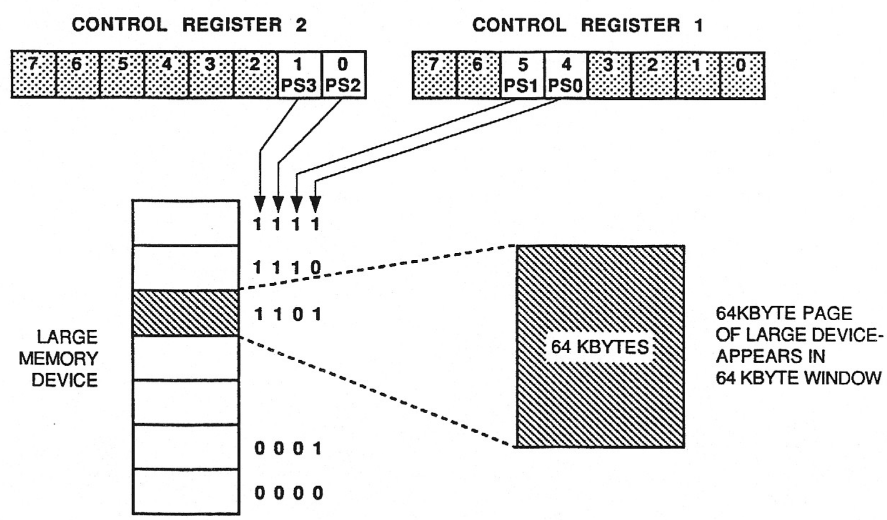

Figure 4-6. Selecting Pages within Large Devices (PS0-3)

Note

The memory window size is 64 Kbytes. Devices containing 32 Kbytes appear at the window address at offset 0 and are duplicated at offset 8000h. Programmers must be aware that BIOS extension programs triggered by 55AAh may reinstall themselves since they might appear more than once in the microprocessor's address space. The optional Ampro XVME-956/101 Support Software will not reinstall itself.

Board Number

The BD0 and BD1 bits in Control Register 1 select the desired module. Each XVME-956/101 module is jumpered for a particular board number, 0 to 3, corresponding to the values of BD0 and BD1. Only one module per control register I/O port address may be jumpered to a given board number. At power up, the control registers of all XVME-956/101 modules are reset to 0.

Multiple XVME-956/101 modules with board number 1, 2, or 3, may be used if they are jumpered for different control register I/O ports. You must be sure the software disables the modules at one I/O address before enabling a module at a different I/O address.

A module jumpered to board number 0 is different. A system may contain, *at most,* one module with Board number 0.

Window Address Selection

The XVME-956/101 unit memory appears in a 64K window at either D0000h or E0000h. The address of the window is jumper selected.

Chapter 5 - 16-Bit Ethernet Installation

Introduction

The XVME-956/411 is a 16-bit Ethernet interface implemented on a PC/104 compatible card. The XVME-956/411 supports 10BaseT (Twisted pair) and 10Base2 (Thin-BNC) Ethernet, plus has an AUI connector for connection to external transceivers. The XVME-956/411 is compatible with the NE2000 or WD8013EBT depending on user configurable EEPROM setup options.

Most XVME-956/411 options are able to be set via a provided setup utility. The two option jumpers available are *8/16 bit bus select* and *10Base2 termination*. Setup options are stored in an on card EEPROM so that the setup utility need only be run when changing hardware settings.

Programmable options include emulation mode NE2000 or WD8013EBT, I/O address, boot PROM enable, boot PROM location, boot PROM size, interrupt select, and 10BaseT / 10Base2 / AUI selection. Selectable interrupts are IRQ2, IRQ3, IRQ4, IRQ5, IRQ10, IRQ11, and IRQ12.

The 10Base2 DC-DC converter can be turned off to minimize power when idle, and is automatically disabled when the XVME-956/411 is setup for twisted pair cable use. The all CMOS design of the XVME-956/411 plus efficient DC-DC converter keeps operating power below 2 watts. Standard packet buffer is 16 Kbytes.

A 32-pin dip socket allows installation of 28 or 32-pin boot PROMs from network vendors. The XVME-956/411 is capable of writing to the boot PROM, allowing use of a 5V flash boot PROM if desired.

Hardware Configuration

The XVME-956/411 has two hardware configuration options: *10Base2 (BNC) termination*, and *8 bit/AUTO bus size selection*. The options are selected with shorting jumpers placed on three pin headers. In the following sections, when the words *"up"*, *"down"*, *"right"*, and *"left"* are used, it is assumed that the XVME-956/411 card is oriented with its bus connectors J1 and J2 at the bottom edge of the card. See Figure 5-1 for jumper locations.

Jumper Settings

Table 5-1. Default Jumper Configuration

Function	Default	Jumper	Position
Termination	Disabled	W1	Down
Bus Size	Auto	W2	Left

Termination

The 10Base2 input (BNC) can be terminated on the XVME-956/411 card. This eliminates the need for the TEE fitting + BNC terminator at the end of the line, and is very convenient for simple two or three node nets. The on-card termination should not be used if the Ethernet cabling is subject to frequent change, as it is easy to forget that a card is terminated internally. The internal termination is enabled by setting the shorting jumper on jumper block W1 in the UP position. Setting the jumper to the DOWN position disables the internal termination.

Bus Size Selection

The XVME-956/411 can work with 8 and 16 bit CPUs. Bus size is normally selected automatically by sensing the voltage on the PC/104 bus J2 connector pin 34. This is a 5V line on the AT part of the bus connector. If 5V is sensed on this line, an AT type CPU is assumed, and 16 bit bus transfers are used.

If the shorting jumper on jumper block W2 is placed in the left hand position, automatic bus sizing is enabled. If the shorting jumper is placed in the right hand position, the XVME-956/411 is forced into the 8 bit mode.

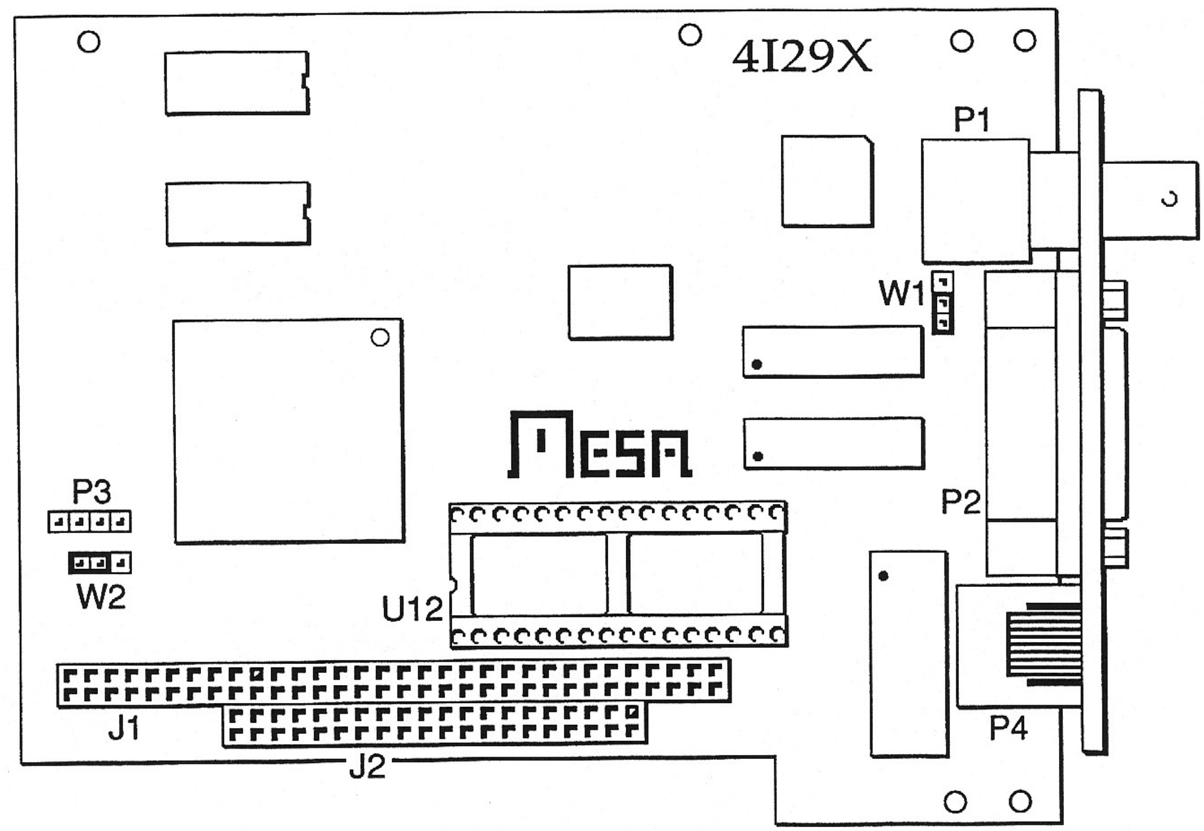

Figure 5-1. Jumper Locations

Installation

After setting jumpers W1 and W2, the XVME-956/411 is ready for installation. It is necessary to install the module on a PC/104 site to perform the software setup. Follow the steps below to install your module:

1. Plug in the Boot ROM chip in U12 (if needed).
2. Install the Ethernet module on the XVME-956 carrier card. Be sure to install the IRQ jumper on the XVME-956 corresponding to the IRQ line the Ethernet module will use.

Software Configuration

Most XVME-956/411 setup options are stored in an on-card EEPROM. This includes the following:

- I/O address
- Interrupt line selection
- Boot PROM enable
- Size
- Location
- Selection of compatibility mode
- Various timing options

Two DOS setup utility programs are supplied with the XVME-956/411. The programs *SET4I29* and *SHOWXVME-956/411* allow you to change these parameters and display the current card setup.

SET4I29

This utility program sets the 4I29 EEPROM options. SET4I29 is invoked with two command line parameters, a port address and a file name:

```
SET4I29  300  WD8013.CFG
```

The port address is 300 the first time SET4I29 is used. The reason is that all 4I29 cards are shipped from Xycom configured for that location, and all port addresses are in hexadecimal. Once a 4I29 card has been configured to a different port address, you need to specify the new port address when running SET4I29.

Because it is possible to forget the port location of a 4I29 card, the port address on the command line can be replaced with 'S'. This causes SET4I29 to look for the 4I29 card by probing all of the possible 4I29 I/O addresses. You should not use the (S)earch option if you know the 4I29 port address, as it is not guaranteed to work in all cases.

The second command line parameter is the name of the configuration file. The configuration file is an ASCII file containing the configuration parameters. The 4I29 distribution disk has two example configuration files, `NE2000.CFG` and `WD8013.CFG`. You should use these files as a starting point to create your own configuration files. The format of the configuration file is very simple—each line of the configuration file consists of a parameter name followed by a parameter value. If a parameter name is not specified in the configuration file, that parameter will be set to the default value shown in Table 5-2.

Table 5- 2. MAINMODE Parameter

Parameter	Parameter Values	Default
MAINMODE	IOMAPPED MEMMAPPED	IOMAPPED

MAINMODE sets the emulation mode of the XVME-XVME-956/411 to I/O mapped (NE2000) or memory mapped (WD8013) operation.

Table 5-3. COMPATIBLE Parameter

Parameter	Parameter Values	Default
COMPATIBLE	Yes No	Yes

If COMPATIBLE is Yes, the buffer mapping matches the standard size and location for WD8013 and NE2000 compatibility. If COMPATIBLE is No, and the XVME-956/411 has 64 Kbytes of buffer RAM, all buffer RAM is accessible.

Table 5- 4. PORTADD Parameters

Parameter	Parameter Values	Default
PORTADD	240 280 2C0 300 320 340 360	300

PORTADD sets the XVME-956/411 I/O port address.

Note

Make sure that no other card in the system uses the same I/O address.

Table 5- 5. INTERRUPT Parameter

Parameter	Parameter Values	Default
INTERRUPT	None IRQ2 IRQ3 IRQ4 IRQ5 IRQ10 IRQ11 IRQ12	None

INTERRUPT selects the interrupt request line that the XVME-956/411 will drive.

Note

Make sure that no other card in the system uses the same interrupt line.

Table 5- 6. PROMLOC Parameter

Parameter	Parameter Values	Default
PROMLOC	None C000-16K C400-16K C800-16K CC00-16K D000-16K D400-16K D800-16K DC00-16K C000-32K C800-32K D000-32K D800-32K C000-64K D000-64K	None

PROMLOC selects the boot PROM location and size. NONE means that the boot PROM is disabled. Make sure that the boot PROM location does not overlap any memory in the system.

Table 5-7.CABLETYPE Parameter

Parameter	Parameter Values	Default
CABLETYPE	TWISTED THIN THICK TWISTEDLOW	TWISTED

CABLETYPE selects the interface type. DC-DC converter is enabled when THIN is selected . TWISTEDLOW uses the twisted pair interface with a lower squelch level for use with longer than normal cables.

Table 5-8. FASTREAD Parameter

Parameter	Parameter Values	Default
FASTREAD	Yes No	No

In I/O mapped mode, FASTREAD causes the next data to be fetched before the previous IORD has completed. Only enable in systems with fast ISA bus.

Table 5- 9.FASTIO16 Parameter

Parameter	Parameter Values	Default
FASTIO16	Yes No	No

If enabled, FASTIO16 causes IOCS16 to be generated by address decode only. If disabled, IOCS16 is generated with IORD and IOWR. (May be needed with some chips.)

Table 5- 10. FASTCHRDY Parameter

Parameter	Parameter Values	Default
FASTCHRDY	Yes No	No

If enabled, IOCHRDY is generated when BALE goes high. If disabled, IOCHRDY is generated with IORD and IOWR.

Note

SET4I29 should be run before any network software has been installed or unpredictable behavior may result. After SET4I29 has been run, you must reset the computer system for the new configuration parameters to take effect. A hardware reset is necessary, *`CONTROL-ALT-DEL`* will not work.

SHOW4I29

This utility program displays some of the current XVME-956/411 setup parameters. The COMPATIBLE option and the PROMLOC option are not readable, so they are not displayed. SHOW4I29 is invoked with the hexadecimal port address on the command line:

SHOW4I29 300

Because it is possible to forget the port location of a XVME-956/411 card, the port address on the command line can be replaced with 'S'. This causes SHOW4I29 to look for the XVME-956/411 card by probing all of the possible XVME-956/411 I/O addresses. You should not use the (S)earch option if you know the XVME-956/411 port address, as it is not guaranteed to work in all cases.

Note

SHOW4I29 should not be run after network software is installed or unpredictable behavior may result.

Default Configuration

The default EEPROM configuration on XVME-956/411 card as shipped from the factory is as follows:

MAINMODE	IOMAPPED
COMPATIBLE	YES
PORTADD	300
INTERRUPT	IRQ5
PROMLOC	NONE
CABLETYPE	THIN
FASTREAD	NO
FASTIO16	NO
FASTCHRDY	NO

Interface Connectors

The paragraphs below describe connectors *10BASE2*, *10BASET,* and *AUI.*

10BASE2

When the BNC connector is used, a BNC TEE must be connected to the XVME-956/411's BNC connector if the Ethernet coax does not end at the XVME-956/411. If the coax ends at the XVME-956/411, a 50 Ohm terminator must be installed. This terminator can be a BNC terminator if the BNC TEE is used or the internal XVME-956/411 termination option can be used.

10BASET

When twisted pair networks are used, a 10BaseT hub must be supplied. You cannot simply connect from one interface card to another when twisted pair is used.

AUI

This connector is provided to external transceivers. This connector is a female D-SUB connector with a pinout that matches the AUI standard pinout. 12 V power on the AUI connector is directly connected to the PC/104 bus 12 V system power.

Specifications

Table 5-11. Electrical Specifications

Characteristic	Specification
Power Requirements Voltage Supply current	 4.5 V (min), 5.5 V (max) +5 V 125mA (max) (AUI, 10BaseT) +5 V 250mA (max) (10Base2)
Bus Loading Input capacitance Input leakage current Output drive capability Output sink current	 15pF (max) 5uA (max) 150pF (min) 12mA (min)

Table 5-12. Environmental Specifications

Characteristic	Specification
Temperature Operating	 -C version 0-70ºC (32ºF to 158ºF)
Humidity Operating	 0-90% RH, non-condensing

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