



## **XPMC-9100**

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Dual PMC Carrier with 8-Port Ethernet Switch

<i>Revision</i>	<i>Description</i>	<i>Date</i>
A	Init	07/07
B	Update	04/08

**Part Number 646710**

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**WARNING**

This is a Class A product. In a domestic environment this product may cause radio interference, in which case the user may be required to take adequate measures.

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European Union Directive 89/336/EEC requires that this apparatus comply with relevant ITE EMC standards. EMC compliance demands that this apparatus is installed within a CompactPCI enclosure designed to contain electromagnetic radiation and which will provide protection for the apparatus with regard to electromagnetic immunity. This enclosure must be fully shielded. An example of such an enclosure is a 6U EMC-RFI CompactPCI System chassis, which includes a front cover to complete the enclosure.

The connection of non-shielded equipment interface cables to this equipment will invalidate European Free Trade Area (EFTA) EMC compliance and may result in electromagnetic interference and/or susceptibility levels that are in violation of regulations which apply to the legal operation of this device. It is the responsibility of the system integrator and/or user to apply the following directions, as well as those in the user manual, which relate to installation and configuration:

All interface cables should be shielded, both inside and outside of the CompactPCI enclosure. Braid/foil type shields are recommended for serial, parallel, and SCSI interface cables. Where as external mouse cables are not generally shielded, an internal mouse interface cable must either be shielded or looped (1 turn) through a ferrite bead at the enclosure point of exit (bulkhead connector). External cable connectors must be metal with metal back-shells and provide 360-degree protection about the interface wires. The cable shield must be terminated directly to the metal connector shell; shield ground drain wires alone are not adequate. CompactPCI panel mount connectors that provide interface to external cables (e.g., RS232, USB, keyboard, mouse, etc.) must have metal housings and provide direct connection to the metal CompactPCI chassis. Connector ground drain wires are not adequate.

## About This Manual

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The Xembedded reference manual provides functional, architectural, and mechanical descriptions of the XCPC-9100. This manual is intended for anyone who designs OEM products which have requirements for PrPMC/PMC Carrier.

## Feedback

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Xembedded welcomes feedback on how we can make our manuals and technical documentation more useful to our customers. Please feel free to send comments and suggestions to [support@xembedded.com](mailto:support@xembedded.com).

## References

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PICMG 2.0 R3.0 ECN2.0-3.0-002  
PICMG 2.3 R1.0  
PICMG 2.6  
PICMG  
c/o Virtual, Inc.  
401 Edgewater Place, Suite 600  
Wakefield, MA 01880, USA  
Phone: 1-781-246-9318  
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# Chapter 1

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## General Description

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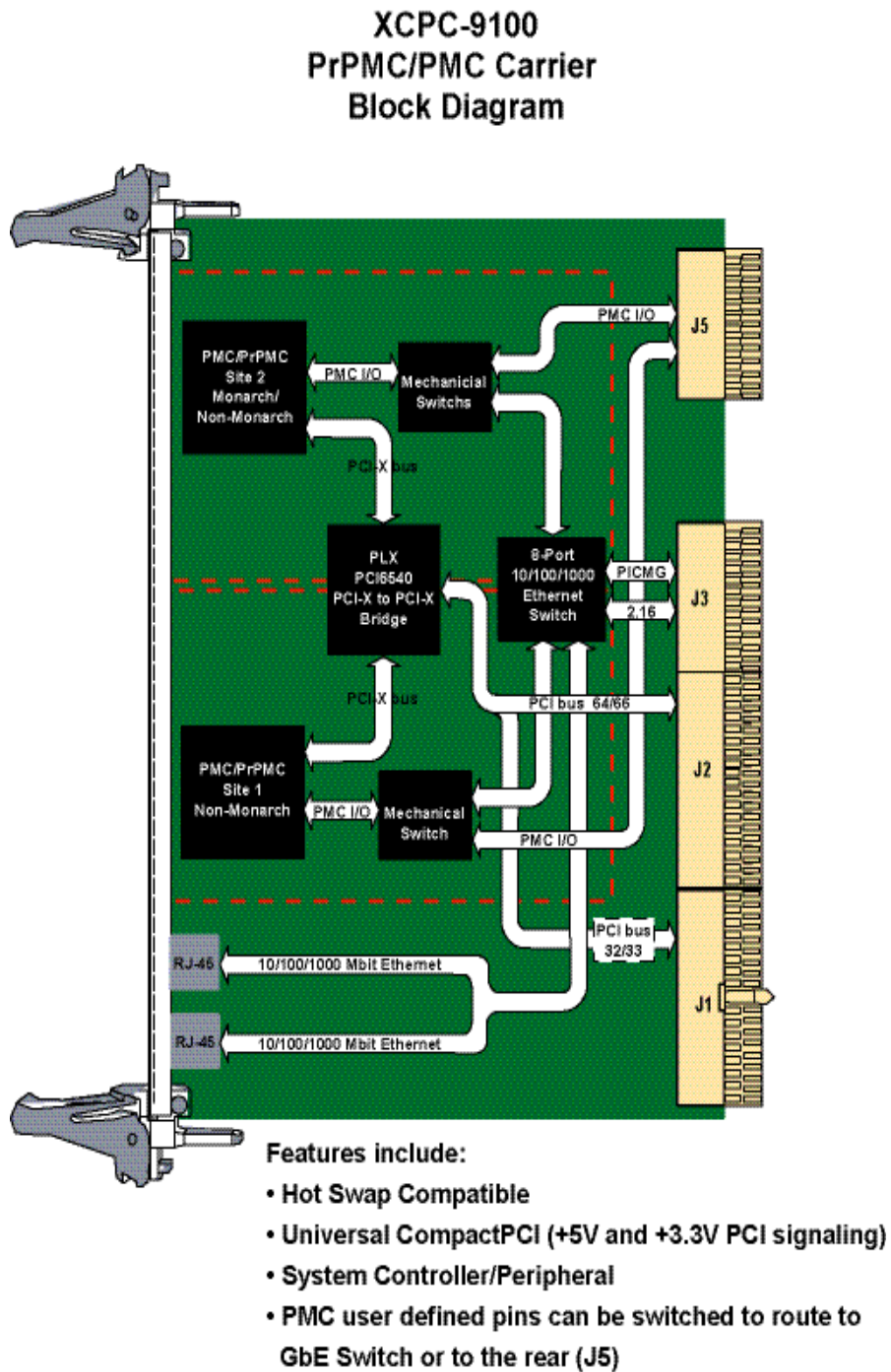
The XCPC-9100 is the most advanced CompactPCI (cPCI) carrier in the market that offers all the features of an eight port switch and can accommodate two PrPMC or PMC modules. The XCPC-9100 switch can be programmed for such features as VLAN. The Carrier can reside in the system controller slot (host slot) or as peripheral slot (agent slot). As the system controller the P2P (PCI to PCI bridge) runs in transparent mode and will configure the cPCI bus. As a peripheral, the P2P bridge runs in non-transparent mode. The Carrier is also compliant to the cPCI 2.16 chassis. In the cPCI 2.16 chassis that do not have the PCI bus routed, the module PCI bus is held in the rest on the secondary side. This allows the two PrPMC/PMC sites to come up independently from the CompactPCI without any adverse effect to either.

In addition the XCPC-9100 has on board an 8-port Gigabit Ethernet (GbE) semi-managed layer two type switch. The switch allows the PrPMC/PMC's that route their GbE to their user define pins on the PMC site J4 connector to be connected directly to the switch. Two ports of the GbE switch are routed to the CompactPCI bus J3 connector per PICMIG 2.16 specification. In addition two ports are routed to the front of the XCPC-9100 Module. Some features of the switch are listed below:

- Fully integrated 10/100/1000Base-T Gigabit Ethernet
- Switch can be reconfigure to provide special functions such as VLAN
- Fully compliant with IEEE 802.3, 802.3u and 802.3ab standards
- Support for jumbo packets up to 9Kbytes
- Full wire speed on all the ports
- Layer two managed (only certain features are supported contact Xembedded Sales)

The XCPC-9100 is hot swappable per cPCI specification with the Blue LED. The XCPC-9100 has an on board micro-controller that report the FRU information to the BMC. The micro-controller is also used to do the management of the switch (i.e. such as VLAN configuration, Mirroring, Rate Limit, etc.). Not all the features of the Layer two managed switch is implement. Contact Xembedded for the list of features.

Figure 1-1 below shows the Architectural of the board.



## XCPC-9100 as the System controller and Peripheral

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The XCPC-9100 utilizes PLX PCI6540 chip for its interface to the cPCI back plane. The chip is a high performance asynchronous 133MHz, 64-bit PCI-X to PCI-X bridge. When the module is in the system controller slot the device runs in transparent P2P bridge. This allows the PrPMC on the Carrier to detect all the devices that on the cPCI chassis.

When the module is in the Peripheral slot, the device run in non-transparent mode. The primary side of the device is the Carrier and secondary side of the P2P is connected to the cPCI back plane. The Primary side which hosts the PrPMC/PMC can run at a different speed vs. the cPCI backplane. This allows the two clock domain to be asynchronous. In this mode the PrPMC slot which is configured to be in the monarch mode (setting is done via the P5 jumper), will configure the Carrier side. The secondary side of the bridge is configured via the cPCI chassis system controller.

### Carrier Interface to the cPCI back plane

In the system controller slot the carrier driver the clock and all the requests/grants to the each of the cPCI slots. The Carrier further routes all the cPCI Interrupts to the Carrier PrPMC. The Carrier can run in cPCI chassis that have +5V or +3.3V PCI signaling. It can also run in PCI-X cPCI chassis.

In the Peripheral slot the bridge is running in non-transparent mode. This allows the system controller on the cPCI to configure the secondary side, however the primary side is configured by the Carrier PrPMC.

In non-transparent mode there are several ways to allow the boot sequencing go through. First the system controller and the Carrier can boot simultaneously (no priority is given). The Carrier requests for 16MB window on it's BAR registers by default (P5 header, remove pin 1-2 and 11-12). In the second case the Carrier must boots first and before the system controller is booted. Installing jumpers on P5 pins 1-2 and 11-12 lets the bridge issue PCI retries on the bus till the Carrier PrPMC release the bridge. Consult the PLX 6540 data book on the registers settings.

### XCPC-9100 as the system controller

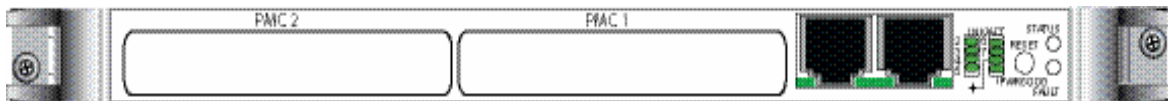
As the system controller the XCP-9100 will try to operate the PCI in PCI-X mode at 66MHz (if the chassis has the capability). The PCI clock will automatically adjust, unless the P5 pin 3-4 or 9-10 is set. When jumper 3-4 is installed the cPCI will clock at max 66MHz in PCI mode. If jumper 9-10 is installed the cPCI bus is forced to run at 33MHz. The slowest peripheral device on the cPCI will dictate the speed of the PCI bus. The clock is automatically adjusted unless the jumpers are set to override.

## Carrier PrPMC/PMC PCI clock speed

The PrPMC/PMC sites of the Carrier run at 133MHz and will adjust their speed according to the PrPMC/PMC module configuration. If both the PrPMC/PMC sites are populated with 133MHz capable PrPMC/PMC the carrier adjust it's speed to 100Mhz. If a single PrPMC/PMC is installed and it can run at 133MHz, the carrier runs at 133MHz. If both the PrPMC/PMC are installed and one of the PrPMC runs slower then 133Mhz, the carrier will adjust it's clock based on the slower clock speed. The Carrier clock speeds can be modified based on P5 Jumper settings 5-6 and 7-8. If jumper 5-6 is installed the Carrier will run at Max speed of 66MHz. If jumper 7-8 is installed the Carrier will run at 33MHz regardless of the capabilities of the PrPMC/PMC.

## PrPMc/PCM PCI signaling

The Carrier PrPMC/PMC sites operate at +3.3 PCI signaling. A PrPMC/PMC which is PCI +5V signaling may damage the Carrier and void the warranty.



Front Panel of the XCPC-9100

### Blue LED

When the XCPC-9100 is placed in a system with an IPMI BMC module the Hot Swap features of the XCPC-9100 are fully functional. At power up and during the insertion the Hot Swap Blue LED comes on and then goes off indicating the board is ready for PCI transactions. During the removal, the handle has to be open, the OS (operating system) will detect the open handle and turn the Blue LED on indicating the module is safe to remove from the system.

### Fault LED

The Fault LED which his Red indicates the voltage on the Carrier are not stable. If the Fault LED is not the module is held in reset

### Link/Activity

There are eight GbE ports from the on-board switch on the carrier. There is a Link/Activity LED associated for each GbE port on the front panel. The two front RJ-45 use their integrated LED for Link/Activity. Only one of the LED on each of the RJ-45 are connected to indicate the Link/Activity. The second LED on the RJ-45 is not connected. The Front panel LED array shows the Link/Activity for the remaining 6 ports of the on-board GbE Switch.

## **Reset Button**

The reset button in the front of the Carrier will reset the carrier. The reset is forwarded to the cPCI chassis if the Carrier is in the system controller slot. In the peripheral slot the reset only reset the two PrPMC/PMC, the Switch Fabric and the PLX P2P bridge Primary side.

## **Reset out from the PrPMC**

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The PrPMC can rest the carrier by issuing the Reset out signal. The Carrier takes that reset and resets the entire module. In the system controller slot this reset is forward to the chassis.

## Main Features

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### Dual 10/100/1000-BaseTX Ethernet to cPCI J3

- The XCPC-9100 has two GbE routed to J3 connector interface per PICMIG 2.16 specification from the on-board switch. The transceivers are fully integrated 10/100/1000BaseT Gigabit Ethernet transceivers. The 10/100/1000-BaseTX Gigabit Ethernet transceivers feature:
  - Fully integrated 10BaseT/100BaseTX and 1000BaseT Gigabit Ethernet
  - Fully compliant with IEEE 802.3, 802.3u and 802.3ab standards
  - Support for jumbo packets up to 9Kbytes

### Dual Port 10/100/1000-BaseTX Ethernet to each PMC site

The XCPC-9100 has a dual port 10/100/1000 Mbps from the on-board switch which is routed to the PMC J4 (user defined pins). Alternately these signals are routed through mechanical switches which allow user defined pins to also go to the J5 Connector (for rear transition module access).

### Dual 10/100/1000-BaseTX Ethernet to Front

The XCPCI-9100 has dual port 10/100/1000-BaseTX routed to the front. This allows the module to run as stand alone without having external switches or a 2.16 switch Fabric in the system.

### Layer Two Semi-Managed Switch

The on board switch Fabric is capable of layer two management. Only certain features are incorporated. The switch can be configured to support Port VLAN programming, see Chapter 3 for more information. Contact Xembedded for other types of custom re-configuration.

### IPMI FRU

The XCPC-9100 uses the NXP LPC2138 micro controller on board for the FRU information. The micro controller communicates with the BMC via the I2C bus and follows the cPCI specification. See appendix A for the layout of the FRU file. The Micro controller also communicates with the GbE switch for it's management portion.

**NOTE:** Please contact Xembedded for the list of features for the Layer two Managed switch.

### PCI Bus interface

The XCPC-9100 uses the PLX-6540 bridge for the PCI bus interface to the cPCI bus. The bridge has the following features:

- PCI R2.3 capable
- PICMG 2.1 Hot swappable
- PCIX 64-bit, 33MHz to 133Mhz PCI clock speed

- Asynchronous operation across the Primary and Secondary (That is the Primary and Secondary can run at two different speed)
- 10KB FIFO
- As the system controller runs in Transparent mode and as a peripheral runs in non-transparent mode
- Support for 8 Bus Masters

## Specifications

The following table is the XCPC-9100 Specifications, showing the recommended operating conditions.

Condition	Recommendation
Compliance	PCI R2.3, PICMG 2.0, PICMG 2.1, PICMG 2.16
Air Flow	200LFM with no PrPMC/PMC installed (air flow is mostly driven by the PrPMC/PMC requirements)
Power	8 Watts while switch running in full wire speed on all the ports.
Operating Temperature	
Storage Temperature	
Relative Humidity	
Operating Altitude	
Non-Operating Altitude	
Shock	
Vibration	
MTBF	

### Safety:

Design to meet or exceed UL 60950 3rd Ed.; CSA C22.2 No.60950-00; EN60950; IEC 60950-a

### EMC:

Design to meet or exceed FCC 47 CFR Part 15, Class B; CE Mark to EN55022/EN55024

Warranty: 2 year limited

## Chapter 2 Installation Guide Introduction

As the CPU technology changes rapidly vs the I/O, the XCPC-9100 allows separation of the CPU from the rest of the I/O subsystem. The XCPC-9100 allows up to two PrPMC/PMC on a carrier. Customers could choose from a variety of PrPMC that are in the Market and also be able to changes the CPU by simply replacing the PrPMC with future faster CPUs.

## XCPC-9100 Mechanical Description

The XCPC-9100 is single slot 6U cPCI module. The unit follows all the specification of the single slot cPCI module. Below figure is the front panel I/O:

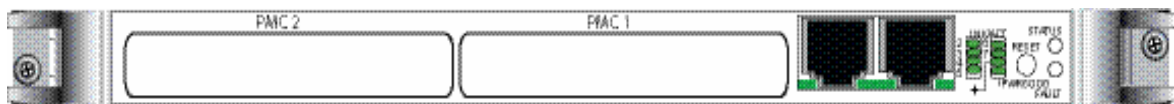


Figure 2-1 Front Panel of the XCPC-9100

## Rear I/O

The XCPC-9100 has rear I/O consisting of the following, see Table 1 below.

Signal	Connector
PCI 32-bit interface PICMG 2.0 R3.0	J1
PCI 64-bit interface PICMG 2.0 R3.0	J2
cPCI 2.16 Dual 10/100/1000-BaseTX	J3
User defined I/O to J5 Per PICMG 2.3 R1.0	J5
IPMI PICMG 2.9	J1 and J2

Table 2-1 XCPC-9100 Rear I/O

# Switches Settings and Locations

The cPCI-9100 has nine switches on board (SW1 and SW9). The settings on switches one to four allows the routing of the PMC site two J4 (user defined I/O) to go to either the GbE switch or the J5 connector of the cPCI. Each of the I/O pins from the PMC is routed to two location on a switch. For example SW1 Pin 16 and Pin 15 is routed to the PMC Site two J4 Pin2. This allows Pin1 and Pin2 two of the switch to be routed to the GbE Switch Fabric on board or the rear I/O J5.

Figure 2-2 XCPC-9100 Switch Settings.

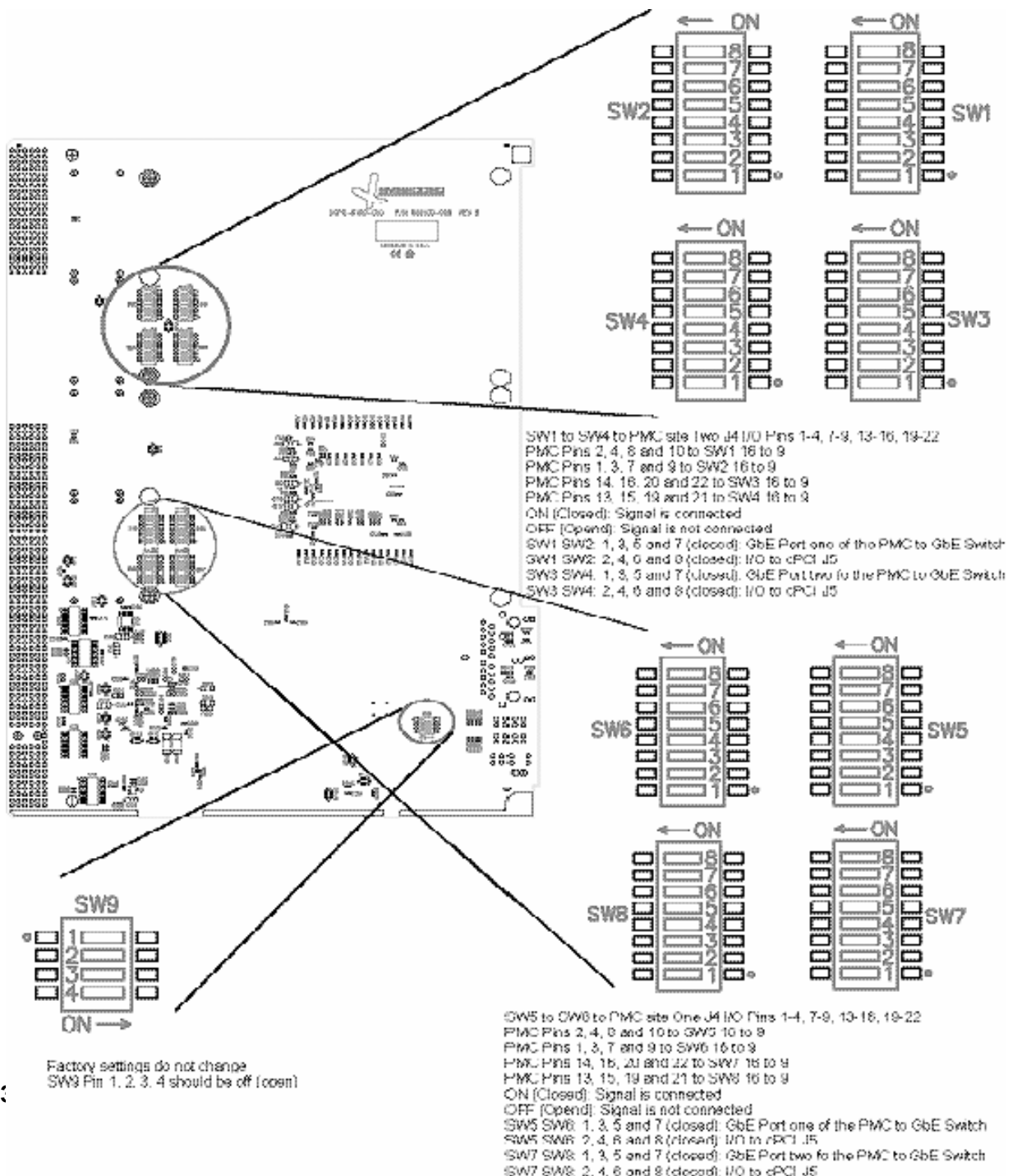


Table 2-2 PMC site Rear I/O switch settings

Switch	Description	
SW1 to SW4	SW1 Pin 16 and 15 to PMC I/O Pin 2	Pin 1, 3, 5 and 7 ON (Closed) signal to GbE Switch
PMC Site Two	SW1 Pin 14 and 13 to PMC I/O Pin 4	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW1 Pin 12 and 11 to PMC I/O Pin 8	GbE Port one of the PMC
	SW1 Pin 10 and 9 to PMC I/O Pin 10	
	SW2 Pin 16 and 15 to PMC I/O Pin 1	Pin 1, 3, 5 and 7 ON (Closed) signal to GbE Switch
	SW2 Pin 14 and 13 to PMC I/O Pin 3	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW2 Pin 12 and 11 to PMC I/O Pin 7	GbE Port one of the PMC
	SW2 Pin 10 and 9 to PMC I/O Pin 9	
	SW3 Pin 16 and 15 to PMC I/O Pin 14	Pin 1, 3, 5 and 7 ON (Closed) signal to GbE Switch
	SW3 Pin 14 and 13 to PMC I/O Pin 16	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW3 Pin 12 and 11 to PMC I/O Pin 20	GbE Port one of the PMC
	SW3 Pin 10 and 9 to PMC I/O Pin 22	
	SW4 Pin 16 and 15 to PMC I/O Pin 13	Pin 1, 3, 5 and 7 ON (Closed) signal to GbE Switch
	SW4 Pin 14 and 13 to PMC I/O Pin 15	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW4 Pin 12 and 11 to PMC I/O Pin 19	GbE Port one of the PMC
	SW4 Pin 10 and 9 to PMC I/O Pin 21	
	SW5 to SW8	SW5 Pin 16 and 15 to PMC I/O Pin 2
PMC Site One	SW5 Pin 14 and 13 to PMC I/O Pin 4	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW5 Pin 12 and 11 to PMC I/O Pin 8	GbE Port one of the PMC
	SW1 Pin 10 and 9 to PMC I/O Pin 10	
	SW2 Pin 16 and 15 to PMC I/O Pin 1	Pin 1, 3, 5 and 7 ON (Closed) signal to GbE Switch
	SW2 Pin 14 and 13 to PMC I/O Pin 3	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW2 Pin 12 and 11 to PMC I/O Pin 7	GbE Port one of the PMC
	SW2 Pin 10 and 9 to PMC I/O Pin 9	
	SW3 Pin 16 and 15 to PMC I/O Pin 14	Pin 1, 3, 5 and 7 ON (Closed) signal to GbE Switch
	SW3 Pin 14 and 13 to PMC I/O Pin 16	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW3 Pin 12 and 11 to PMC I/O Pin 20	GbE Port one of the PMC
	SW3 Pin 10 and 9 to PMC I/O Pin 22	
	SW4 Pin 16 and 15 to PMC I/O Pin 13	Pin 1, 3, 5 and 7 ON (Closed) signal to GbE Switch
	SW4 Pin 14 and 13 to PMC I/O Pin 15	Pin 2, 4, 6 and 8 ON (Closed) signal to cPCI J5
	SW4 Pin 12 and 11 to PMC I/O Pin 19	GbE Port one of the PMC
	SW4 Pin 10 and 9 to PMC I/O Pin 21	
	SW9	Factory Settings

**NOTE:** The signal for the PMC I/O J4 should either be routed to the cPCI J5 or to the on board GbE switch Fabric. For example closing (ON position) for the SW1 Pin1 and Pin2 is not allowed. Depending on the I/O which is on the PMC, routing to both the cPCI J5 and GbE Ethernet switch may damage the module.

## XCPC-9100 Installation into rack

The XCPC-9100 can be installed in a standard cPCI 32-bit or 64-bit PCI bus. Also cPCI 2.16 style chassis without a PCI bus interface or 2.16 chassis with the PCI bus interface could be used. Installation Procedure:

**NOTE:** Configure the Switch setting SW1 to SW8 according to the PMC module being installed. Notice the PMC I/O should only route to the on board GbE or the cPCI J5, but not both. Configure P5 jumper header, depending on the PMC modules being installed.

1. Configure and install the PrPMC/PMC according to the manufacturer's suggested installation procedure. Tighten the four screws per PMC.
2. Configure P5 such that only one of the PMCs is running in Monarch Mode. Only one PMC should be configured as Monarch. If Both PMC is configured as Monarch the result is unpredictable. However, both PMC could run as Agent (non-Monarch).
3. With the solder side facing up on the carrier (depending on the chassis), Slide the XCPC-9100 into the chassis. Press firmly on the board until the connectors are fully mated. Tighten the front screws ensuring that the carrier is secured to the backplane.

**WARNING:** Make sure the front handles are closed firmly or the hot switch which is integrated in the lower handle may not turn the board on.

4. Installation is complete, power up the board.

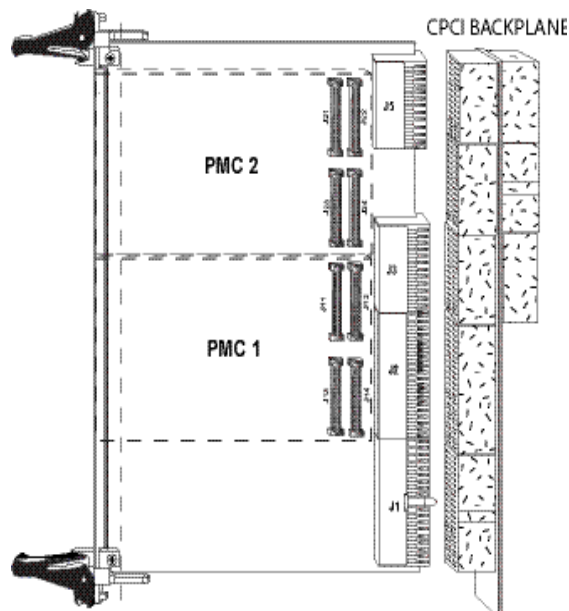


Figure 2-3 Typical Installation

## PMC Connectors

There are eight PMC connectors on the carrier. Connectors J21, J22, J23, J24 corresponds to the PMC connectors P1, P2, P3 and P4 for PMC site two. Connectors J11, J12, J13 and J14 corresponds to the PMC connectors P1, P2, P3 and P4 for PMC site one.

Pin No	Signal	Pin No	Signal
1	N/C	2	N/C
3	GND	4	*PCI_INTA
5	*PCI_INTB	6	*PCI_INTC
7	*PRESENT	8	+5V
9	*PCI_INTD	10	N/C
11	GND	12	N/C
13	PCI_CLK	14	GND
15	GND	16	PCI_GNT1
17	*PCI_REQ1	18	+5V
19	+3.3V	20	PCI_AD31
21	PCI_AD28	22	PCI_AD27
23	PCI_AD25	24	GND
25	GND	26	PCI_C1BE3
27	PCI_AD22	28	PCI_AD21
29	PCI_AD19	30	+5V
31	+3.3V	32	PCI_AD17
33	*FRAME	34	GND
35	GND	36	*PCI_IRDY
37	*PCI_DEVSEL	38	+5V
39	PCI_PCIXCAD	40	N/C
41	N/C	42	N/C
43	PCI_PWR	44	GND
45	+3.3V	46	PCI_AD15
47	PCI_AD12	48	PCI_AD11
49	PCI_AD09	50	+5V
51	GND	52	PCI_C1BE0
53	PCI_AD06	54	PCI_AD05
55	PCI_AD04	56	GND
57	+3.3V	58	PCI_AD03
59	PCI_AD02	60	PCI_AD01
61	PCI_AD00	62	+5V
63	GND	64	*PCI_REQ4

Table 2-3 Pin out for the J21 and J11.

Table 2-4 showing pin out of the J22 and J12

Pin No.	Signal	Pin No.	Signal
1	N/C	2	N/C
3	N/C	4	TD0
5	TD1	6	GND
7	GND	8	N/C
9	N/C	10	N/C
11	N/C	12	+3.3V
13	*PCI_RST	14	N/C
15	+3.3V	16	N/C
17	*PCI_PME	18	GND
19	PCI_AD30	20	PCI_AD29
21	GND	22	PCI_AD26
23	PCI_AD18	24	+3.3V
25	PCI_IDSEL	26	PCI_AD23
27	+3.3V	28	PCI_AD20
29	PCI_AD18	30	GND
31	PCI_AD16	32	*PCI_C/BE2
33	GND	34	IDSELB
35	*PCI_TRDY	36	+3.3V
37	GND	38	*PCI_STOP
39	*PCI_PERR	40	GND
41	+3.3V	42	*PCI_SERR
43	*PCI_C/BE1	44	GND
45	PCI_AD14	46	PCI_AD13
47	PCI_M66EN	48	PCI_AD10
49	PCI_AD08	50	+3.3V
51	PCI_AD07	52	*REQB
53	+3.3V	54	*GNTB
55	N/C	56	GND
57	N/C	58	ERREADY
59	GND	60	*RSTOUT
61	*PCI_ACK64	62	+3.3V
63	GND	64	*MONARCH

Table 2-5 Pin out for the J23 and J13

Pin No.	Signal	Pin No.	Signal
1	N/C	2	GND
3	GND	4	PCI_CBE7
5	PCI_CBE6	6	PCI_CBE5
7	PCI_CBE4	8	GND
9	+3.3V	10	PCI_PAR64
11	PCI_AD63	12	PCI_AD62
13	PCI_AD61	14	GND
15	GND	16	PCI_AD60
17	PCI_AD59	18	PCI_AD58
19	PCI_AD57	20	GND
21	+3.3V	22	PCI_AD56
23	PCI_AD55	24	PCI_AD54
25	PCI_AD53	26	GND
27	GND	28	PCI_AD52
29	PCI_AD51	30	PCI_AD50
31	PCI_AD49	32	GND
33	GND	34	PCI_AD48
35	PCI_AD47	36	PCI_AD46
37	PCI_AD45	38	GND
39	+3.3V	40	PCI_AD44
41	PCI_AD43	42	PCI_AD42
43	PCI_AD41	44	GND
45	GND	46	PCI_AD40
47	PCI_AD39	48	PCI_AD38
49	PCI_AD37	50	GND
51	GND	52	PCI_AD36
53	PCI_AD35	54	PCI_AD34
55	PCI_AD33	56	GND
57	+3.3V	58	PCI_AD32
59	N/C	60	N/C
61	N/C	62	GND
63	GND	64	N/C

Table 2-6 Pin Out definition for J24 from PMC site 2.

Pin No.	Signal	CPCI J5 or GbE Switch*	Pin No.	Signal	CPCI J5 or GbE Switch*
1	I/O1	TRD0-/1; E22	2	I/O2	TRD2+/1; D22
3	I/O3	TRD0-/1; C22	4	I/O4	TRD2-/1; B22
5	I/O5	A22	6	I/O6	E21
7	I/O7	TRD1-/1; D21	8	I/O8	TRD3+/1; C21
9	I/O9	TRD1-/1; B21	10	I/O10	TRD3-/1; A21
11	I/O11	E20	12	I/O12	D20
13	I/O13	TRD0-/2; C20	14	I/O14	TRD2+/2; B20
15	I/O15	TRD0-/2; A20	16	I/O16	TRD2-/2; E19
17	I/O17	D19	18	I/O18	C19
19	I/O19	TRD1-/2; B19	20	I/O20	TRD3+/2; A19
21	I/O21	TRD1-/2; E18	22	I/O22	TRD3-/2; D18
23	I/O23	C18	24	I/O24	B18
25	I/O25	A18	26	I/O26	E17
27	I/O27	D17	28	I/O28	C17
29	I/O29	B17	30	I/O30	A17
31	I/O31	E16	32	I/O32	D16
33	I/O33	C16	34	I/O34	B16
35	I/O35	A16	36	I/O36	E15
37	I/O37	D15	38	I/O38	C15
39	I/O39	B15	40	I/O40	A15
41	I/O41	E14	42	I/O42	D14
43	I/O43	C14	44	I/O44	B14
45	I/O45	A14	46	I/O46	E13
47	I/O47	D13	48	I/O48	C13
49	I/O49	B13	50	I/O50	A13
51	I/O51	E12	52	I/O52	D12
53	I/O53	C12	54	I/O54	B12
55	I/O55	A12	56	I/O56	E11
57	I/O57	D11	58	I/O58	C11
59	I/O59	B11	60	I/O60	A11
61	I/O61	E10	62	I/O62	D10
63	I/O63	C10	64	I/O64	B10

Table 2-7 for the pin out of the J14 Rear I/O for PMC site 1.

Pin No.	Signal	CPCI J5 or GbE Switch*	Pin No.	Signal	CPCI J5 or GbE Switch*
1	I/O1	TRD0+/3; E9	2	I/O2	TRD2+/3; D9
3	I/O3	TRD0-/3; C9	4	I/O4	TRD2-/3; B9
5	I/O5	A9	6	I/O6	E8
7	I/O7	TRD1+/3; D8	8	I/O8	TRD3+/3; C8
9	I/O9	TRD1-/3; B8	10	I/O10	TRD3-/3; A8
11	I/O11	E7	12	I/O12	D7
13	I/O13	TRD0+/4; C7	14	I/O14	TRD2+/4; B7
15	I/O15	TRD0-/4; A7	16	I/O16	TRD2-/4; E6
17	I/O17	D6	18	I/O18	C6
19	I/O19	TRD1+/4; B6	20	I/O20	TRD3+/4; A6
21	I/O21	TRD1-/4; E5	22	I/O22	TRD3-/4; D5
23	I/O23	C5	24	I/O24	B5
25	I/O25	A5	26	I/O26	E4
27	I/O27	D4	28	I/O28	C4
29	I/O29	B4	30	I/O30	A4
31	I/O31	E3	32	I/O32	D3
33	I/O33	C3	34	I/O34	B3
35	I/O35	A3	36	I/O36	E2
37	I/O37	D2	38	I/O38	C2
39	I/O39	B2	40	I/O40	A2
41	I/O41	E1	42	I/O42	D1
43	I/O43	C1	44	I/O44	B1

## Backplane CompactPCI Connectors

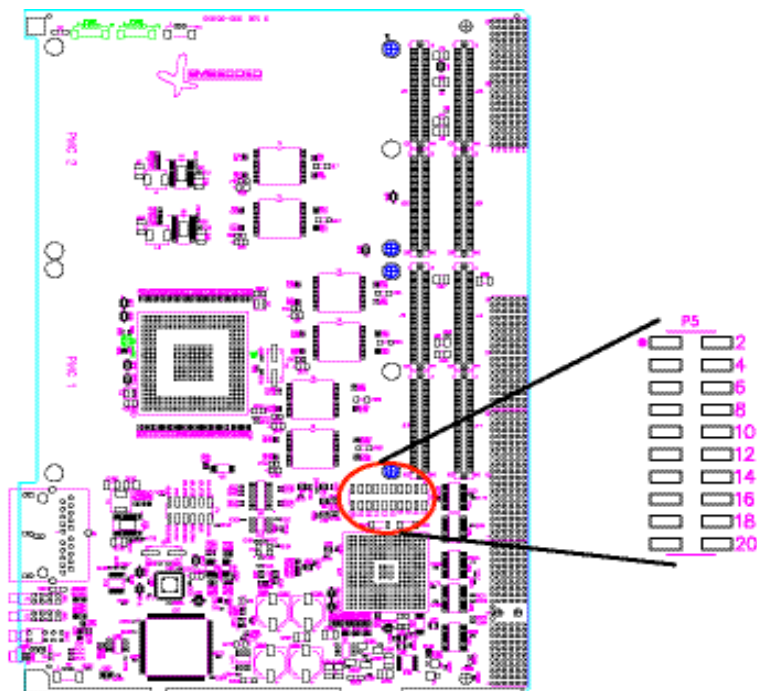
Backplane connectors J1, J2 and J3 follow the PICMG 2.0 Release3.0 pin out. The J3 connector follows the cPCI PICMG 2.16 specification when switches are configured to place two 10/100/1000 Ethernet ports from the on-board switch. The other position of the configuration switch configures the XCPC-9100 to route the rear PMC I/O to J5 of the CompactPCI backplane.

Table 2-8 CompactPCI backplane signals

32	GND	GA4	GA3	GA2	GA1	GA0	GND	
31	GND	CLK2	GND	RSV	RSV	RSV	GND	
30	GND	CLK3	GND	RSV	GND	RSV	GND	
29	GND	GND	GND	RSV	RSV	RSV	GND	P2
18	GND	BR5VP2A16	BR5VP2B16	BR5VP2C16	GND	BR5VP2E16	GND	F
17	GND	BR5VP2A17	GND	PRST#	RDQ#	GHT#	GND	J2
16	GND	BR5VP2A16	BR5VP2B16	DEG#	GND	BR5VP2E16	GND	
15	GND	BR5VP2A15	GND	FAU#	RDQ#	GHT#	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[34]	GND	VV0#	AD[37]	AD[36]	GND	C
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[38]	GND	O
11	GND	AD[41]	GND	VV0#	AD[44]	AD[43]	GND	H
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	H
9	GND	AD[57]	GND	VV0#	AD[51]	AD[50]	GND	E
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	C
7	GND	AD[58]	GND	VV0#	AD[59]	AD[57]	GND	T
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	O
5	GND	C/BE[5]#	GND	VV0#	C/BE[4]#	PAR#	GND	R
4	GND	VV0#	BR5VP2B4	C/BE[7]#	GND	C/BE[6]#	GND	
3	GND	CLK4	GND	GHT#	RDQ#	GHT#	GND	
2	GND	CLK3	CLK3	SYSTEM#	GHT#	RDQ#	GND	
1	GND	CLK1	GND	RDQ#	GHT#	RDQ#	GND	
35	GND	5V	REQ#	ENUM#	3.3V	5V	GND	
34	GND	AD[5]	5V	VV0#	AD[6]	ACK#	GND	
33	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
32	GND	AD[7]	GND	3.3V	AD[8]	AD[5]	GND	P1
31	GND	3.3V	AD[9]	AD[8]	MEM#	C/BE[3]#	GND	F
30	GND	AD[12]	GND	VV0#	AD[11]	AD[10]	GND	J1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	SDO#	SDO#	GND	PERR#	GND	
16	GND	DEVSEL#	GND	VV0#	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	O
13-14	KEY AREA							
11	GND	AD[16]	AD[17]	AD[18]	GND	C/BE[2]#	GND	H
10	GND	AD[21]	GND	3.3V	AD[20]	AD[18]	GND	E
9	GND	C/BE[3]#	IOSEL	AD[23]	GND	AD[22]	GND	C
8	GND	AD[25]	GND	VV0#	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	RDQ#	GND	3.3V	CLK	AD[31]	GND	R
5	GND	BR5VP1A5	BR5VP1B5	RST#	GND	GNT#	GND	
4	GND	BR5VP1A4	GND	VV0#	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK	5V	TMS	TDO	TDI	GND	
1	GND	5V	-12V	TRST#	+12V	5V	GND	
Pin	Z	A	B	C	D	E	F	

## Jumper Header P5

Figure 2-4 jumper header P5 is located on the top side of the board as shown below.



### Jumper P5:

Pin	Open	Closed
1 – 2	Carrier boot priority	cPCI Boot Priority
3 – 4	cPCI PCI-X auto select	cPCI is PCI
5 – 6	Carrier PCI-X auto select	Carrier is PCI
7 – 8	Carrier PCI speed auto select	Carrier 33MHz
9 – 10	cPCI speed is auto select	cPCI 33MHz
11 – 12	Secondary BAR16MB Window	Carrier will select
13 – 14	PMC1 is Monarch	PMC1 is not Monarch
15 – 16	PMC2 is Monarch	PMC2 is not Monarch
17 – 18	N/C	
19 – 20	Leave Open	

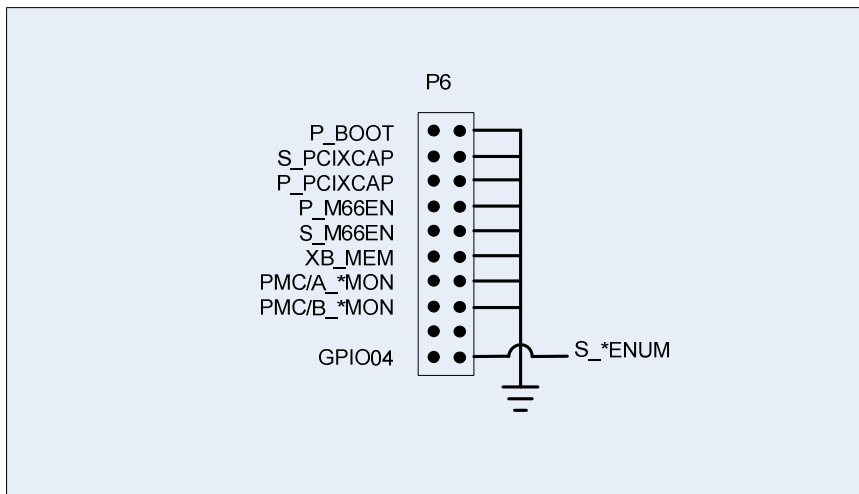
## XCPC-9100 Switch and Header Information

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### Option Header (P6)

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The following signals are set via jumpers on the 20-Pin Option Header designated



<b>Signal</b>	<b>Definition</b>
<b>P_BOOT</b>	Primary Port Boot Priority. Add Jumper to give secondary port boot priority in Non-Transparent mode
<b>S_PCIXCAP</b>	Secondary Bus PCI-X Capability. Add Jumper if Secondary PCI Bus is Not PCI-X capable
<b>P_PCIXCAP</b>	Primary Bus PCI-X Capability Pin. Add Jumper if Primary PCI Bus is Not PCI-X capable
<b>P_M66EN</b>	Primary Bus 66 MHz Enable Add Jumper if Primary PCI Bus is Not Capable of 66 MHz operation
<b>S_M66EN</b>	Secondary Bus 66 MHz Enable Add Jumper if Secondary PCI Bus is Not Capable of 66 MHz operation
<b>XB_MEM</b>	Cross-Bridge Memory Enable. Remove Jumper to allow the PCI Bridge to claim 16 MB of memory and allow lower priority boot ports to proceed without waiting for the Base Address Registers to be programmed
<b>PMC/A_*MON</b>	PMC-A Monarch Mode Add Jumper if PMC-A is to be set as monarch. Leave open otherwise
<b>PMC/B_*MON</b>	PMC-B Monarch Mode Add Jumper if PMC-B is to be set as monarch. Leave open otherwise
<b>GPIO04</b>	Add Jumper to connect secondary bus *ENUM signal to the GPIO04 pin of the This signal is used as part of the Hot-Swap mechanism to ensure proper enumeration of a newly inserted board

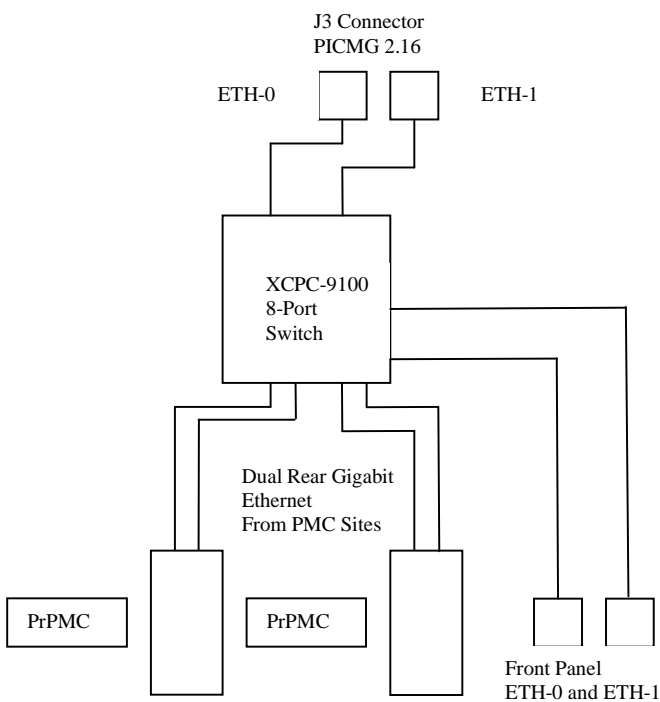
## Chapter 3 Ethernet Switch Setup and VLAN Configuration

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### The On-Board Switch

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The XCPC-9100 includes an on-board 8-port Level-2, 10/100/1000Mbps Ethernet Switch. The XCPC-9100 has two Ethernet ports on the front panel, two ports out the CompactPCI J3 backplane connector for PICMG 2.16 support and dual Ethernet ports out J14 on PMC site 1 and dual Ethernet ports out J24 on PMC site 2 when using the XPMC-6710 PowerPC PMC processor module. This on-board switch reduces the amount of space required in a rack to achieve a robust system in a smaller footprint. The switch can be programmed using the IPMI micro Controller and on-board software for a number of different uses including normal operation and Port Based VLAN.



### What is VLAN Support?

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The IEEE 802.1q specification was expanded to include VLAN (virtual LAN) headers for IPMI over IP sessions on IEEE 802.3 Ethernet. VLAN works with VLAN-aware routers and switches such as the XCPC-9100 to allow a physical network to be partitioned into 'virtual' networks where a group of devices on different physical LAN segments can communicate with each other

as if they were all on the same physical LAN segment. This can be used to group classes of network membership at the Ethernet Packet level rather than at the IP level, as might be done with a router. VLAN allows system administrators to 'management VLAN' where only members of that VLAN will receive packets related to management, and, conversely, will be isolated from the need to process network traffic for other VLANs. This adds a higher level of access to the resources a diverse group within a company to work together virtually with common shared network resources.

## Why Use VLANs?

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- Security—Separation of systems with sensitive data from the rest of the network provides security. This system separation decreases the chance that someone can gain access to information that the person does not have authorization to see.
- Projects/special applications—simplify the management of a project or work group using a special application with VLAN. VLAN brings all the necessary nodes together allowing shared network resources and project management. C
- Performance/bandwidth—The network administrator can create VLANs that reduce the number of router hops. The VLANs can also increase the effective network bandwidth for users.
- Broadcasts/traffic flow—Since VLANs do not pass broadcast traffic to nodes that are not part of the VLAN, a VLAN automatically reduces broadcasts.
- Departments/specific job types—Set up VLANs for departments that are heavy network users, such as multimedia or engineering departments. VLANs can be setup across department lines with dedicated VLANs to specific types of employees, such as managers or salespeople.

You can create up to 4 VLANs with the Xembedded XCPC-9100 on-board Level-2 managed switch using the procedure shown below.

While you can have more than one VLAN on the XCPC-9100 switch, each VLANs cannot communicate directly with each other. This would defeat the purpose of a VLAN, which is to isolate a part of the network. Communication between VLANs requires the use of a router.

## Procedure for VLAN set-up.

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The following equipment is required and used to complete this procedure:

- A XCPC-9100 3 pin to DB-9 serial cable. This cable connects RS-232, data leads only from PC work Station to P3 on the XCPC-9100.

## XCPC-9100

- A XCPC-9100 configured for PMC site Ethernet to the on-board switch (XCPC-9100 switches 1-8 with ODD numbered switches on and all others off).
- Two XPMC-6710s with both Ethernet ports configured to the back P4 connector. This is configured via the SW3, position 1 and 4 ON and all others OFF.
- PC work Station capable of running a terminal program with Communication port set to 115.2K baud rate.
- CompactPCI, PICMG 2.16 Chassis with a Switch Fabric board to monitor the PICMG 2.16 channels from the XCPC-9100.

## VLAN CONFIGURATION

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- Make sure SW9 on the XCPC-9100, position 3 is off.
- Plug the 3pin to DB-9 serial cable from the PC work station to P3 on the XCPC-9100. P3 is keyed but be sure to observe pin1 for this connection.
- Insert XCPC-9100 with two XPMC-6710 modules into the CompactPCI chassis and power up.
- Using a terminal emulation application, set port to 115200 baud rate, 8-bit, N0 parity and 1 stop bit, No flow control.
  
- Power on the Chassis.
- On the computer screen you should see the following message:
  - SPI Interface Established
- Hitting any key it will take you to this menu:
  - Xembedded Main Menu
  - Port-Based VLAN Configuration
    - Note: up to four VLANs can be configured on the XCPC-9100.*
- Select 1. You will get this sub menu:
  - 0-3) Port-Based VLAN Configuration
    - d) Display VLAN Configuration
    - w) Write configuration to Flash
    - x) Exit to Main Menu
  
  - Selecting 0 to 3 will let you enter in ports to put with that VLAN. Format for inputting is port numbers with a space between each number. This is the list of numbers that correspond to which port:
    - 0 - Front port 0 of XCPC-9100
    - 1 - Front port 1 of XCPC-9100
    - 2 – PMC site 1 port eth0
    - 3 – PMC site 1 port eth1
    - 4 – PMC site 2 port eth0
    - 5 – PMC site 2 port eth1
    - 6 - To CPCI J3
    - 7 - To CPCI J3

## XCPC-9100

*NOTE: To route the Ethernet PMC ports to the on-board Ethernet switch, SW1 to SW8 on the XCPC-9100 must be set with all odd positions ON and all even positions OFF.*

*If you don't assign all ports to a VLAN the unassigned ports go to an unassigned location and are not routed.*

- k. Selecting menu item 'w' permanently writes the configuration to flash. When selected, it will give a response confirming configuration was saved.
- l. Selecting menu item 'd' will display the current VLAN configuration. (Note in Minicom, use SHIFT+Page Up to scroll up the screen) Default configuration is ports 0 thru 7 part of VLAN 0 and all other VLANs empty. Verification should be done to assure module is setup correctly.
- m. Selecting menu item 'x' will take you to the top Xembedded menu.
- n. When done power off the chassis.
  - o. Remove the XCPC-9100, setup is complete.

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## Chapter 4 IPMI Controller

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The IPMI controller on the XCPC-9100 works as an IPM (Intelligent Platform Management) The FRU Information is used primarily to provide 'inventory' information about this board in the CompactPCI Chassis. The FRU will provide the Supplier's name, Xembedded, part number, 609100-001 and version number(s), Rev 1.3. These items can be read through the system IPMI software.

The XCPC-9100 uses an on-board micro controller for the IPMI function to support FRU (Field Replaceable Unit) information per the IPMI 1.5 specification. This function supplies the BMC (Base Management Controller) on the System Controller board with the information to replace the XCPC-9100. The on-board IPMI controller receives requests for this table information with the following commands and responses.

### FRU Inventory Area Information

---

This command is used to obtain information about the size and access method of the FRU Inventory data on the XCPC-9100.

NetFn 0x0A, Cmd 0x10

	Byte	Value	Data Field
Request-Data	1	XX <sub>h</sub>	FRU device ID,
Response-data	1	00 <sub>h</sub>	Completion code
	2	XX <sub>h</sub>	FRU inventory area size in bytes, lower byte
	3	XX <sub>h</sub>	FRU inventory area size in bytes, High byte
	4	XX <sub>h</sub>	[7:1] – reserved [0] – 0b = accessed by bytes 1b = accessed by bytes

## Read FRU Data

This command returns the specified data from the FRU Inventory information area. No parsing of the FRU data is performed by the IPMI subsystem; System management software is responsible for interpreting the FRU data.  
NetFn 0x0A, Cmd 0x10

	Byte	Value	Data Field	Comments
Request-Data	1	XX <sub>n</sub>	FRU device ID,	
	2	XX <sub>n</sub>	FRU Inventory offset to read Low Byte	
Completion code	3	XX <sub>n</sub>	FRU inventory area size in bytes, High byte	Offset is in words or bytes per device access type returned in the FRU Inventory Area information command.
Response-data	4	XX <sub>n</sub>	Count to read – 1 based	
	1	00 <sub>n</sub>	Completion code	
	2	XX <sub>n</sub>	Count returned – 1 based	
	3-2+N		Requested data	

The XCPC-9100 comes with FRU preloaded.

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## Write FRU Data

This command writes the specified byte or word to the FRU Inventory Information area. No parsing of the FRU data is performed by the IPMI subsystem management software is responsible for creating valid FRU data structures and writing the data to the FRU area.

NetFn 0x0A, Cmd 0x10

	Byte	Value	Data Field	Comments
Request-Data	1	XX <sub>n</sub>	FRU device ID,	
	2	XX <sub>n</sub>	FRU Inventory offset to read Low Byte	
	3	XX <sub>n</sub>	FRU inventory area size in bytes, High byte	Offset is in words or bytes per device access type returned in the FRU Inventory Area information command.
Response-data	4:3+N	XX <sub>n</sub>	Data to Write	
	1	00 <sub>h</sub>	Completion code 00 <sub>h</sub> - Successful 80 <sub>h</sub> - Write Protected	
	2	XX <sub>n</sub>	Count returned – 1 based	

## FRU Data Specification

The XCPC-9100 is pre-loaded with the following data at the factory.

### Board Information:

Product : "CPC"  
File ID : "MgtCtrl.bin"  
Part : "CPC 9100"  
Serial : <varies>  
Manuf. : "Xembedded"

### Product Information:

Product : "CPC"  
Version : "01.01"  
Part : "609100"  
Manuf ID: "0x029117"  
Manuf. : " Xembedded "